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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD
B	0003279770	PRODUCTION RELEASED	2014-09-29

MLB B - PVT

LAST_MODIFIED=Mon Sep 29 18:09:18 2014

RADIO_MLB SYNC VER 0.109.0
WIFI_DEV SYNC VER 0.68.0
ROTTERDAM SYNC VER 0.11.0

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	TABLE OF CONTENTS	N/A	N/A
2	2	BLOCK DIAGRAM: SYSTEM	N/A	N/A
3	4	BOM TABLES	N/A	N/A
4	5	SOC: MISC & ALIASES	N/A	N/A
5	6	SOC: MAIN	N/A	N/A
6	7	SOC: I/OS	N/A	N/A
7	8	SOC: NAND	N/A	N/A
8	9	SOC: MIPI, ISP	N/A	N/A
9	10	SOC: EDP, PCIE	N/A	N/A
10	11	SOC: DDR	N/A	N/A
11	12	SOC: IO POWER	N/A	N/A
12	13	SOC: SOC POWER AND GND	N/A	N/A
13	14	SOC: CPU, GPU, SRAM POWER	N/A	N/A
14	16	DDR: CHANNEL 0 AND 1	N/A	N/A
15	17	DDR: CHANNEL 2 AND 3	N/A	N/A
16	18	NAND	N/A	N/A
17	20	SENSOR: OSCAR	N/A	N/A
18	21	SENSOR: CARBON, PHOS+, MAGN	N/A	N/A
19	22	SENSOR: HALL EFFECT	N/A	N/A
20	27	CAMERA: CAM CONNS	N/A	N/A
21	28	CAMERA: CAM SUPPORT	N/A	N/A
22	30	AUDIO: L81 CODEC	N/A	N/A
23	31	AUDIO: HP/DMIC FLEX CONNS	N/A	N/A
24	32	AUDIO: SPEAKER AMPS	N/A	N/A
25	35	IO: TRISTAR	N/A	N/A
26	36	IO: FILTERS	N/A	N/A
27	37	IO: HOTBAR PADS	N/C	N/A
28	39	IO: BUTTON FLEX CONN	N/A	N/A
29	40	GRAPE: STINGER & CONN	N/A	N/A
30	41	GRAPE: CUMULUS	N/A	N/A
31	45	DISPLAY: CONNECTOR	N/A	N/A
32	46	DISPLAY: EDP SUPPORT	N/A	N/A
33	47	MESA: SUPPORT	N/A	N/A
34	48	ROTTERDAM	ROTTERDAM	05/13/2014
35	50	CELL: PROBE PTS & DEBUG CONN	RADIO	09/29/2014
36	51	CELL: BB PMU (1/2)	RADIO	09/29/2014
37	52	CELL: BB PMU (2/2)	RADIO	09/29/2014
38	53	CELL: BASEBAND (1/2)	RADIO	09/29/2014
39	54	CELL: BASEBAND (2/2)	RADIO	09/29/2014
40	55	CELL: BASEBAND (3/3)	RADIO	09/29/2014
41	56	CELL: RF TXCVR (1/3)	RADIO	09/29/2014
42	57	CELL: RF TXCVR (2/3)	RADIO	09/29/2014
43	58	CELL: RF TXCVR (3/3)	RADIO	09/29/2014
44	59	CELL: QFE DCDC	RADIO	09/29/2014
45	60	CELL: 2G PA	RADIO	09/29/2014
46	61	CELL: VLB PAD	RADIO	09/29/2014
47	62	CELL: LB PAD	RADIO	09/29/2014
48	63	CELL: MB PAD	RADIO	09/29/2014
49	64	CELL: HB PAD	RADIO	09/29/2014
50	65	CELL: ANTENNA SWITCH	RADIO	09/29/2014
51	66	CELL: HB SWITCH	RADIO	09/29/2014
52	67	CELL: RX DIV (1/2)	RADIO	09/29/2014
53	68	CELL: RX DIV (2/2)	RADIO	09/29/2014
54	69	CELL: GPS	RADIO	09/29/2014
55	70	CELL: ANT FEEDS & GPS (J82)	RADIO	09/29/2014
56	74	WIFI/BT: J82 ANT INTERFACE	WIFI	09/29/2014
57	75	WIFI/BT: WIFI/BT MODULE	WIFI	09/29/2014
58	78	SENSOR: HAMMERHEAD	N/A	N/A
59	79	CELL: SIM AND ANT SW FILT	N/A	N/A
60	81	PMU: ARABELA (1/3)	N/A	N/A
61	82	PMU: ARABELA (2/3)	N/A	N/A
62	83	PMU: ARABELA (3/3)	N/A	N/A
63	84	POWER: J82 SPECIFIC	N/A	N/A
64	86	POWER: EXTERNAL SWITCHES	N/A	N/A
65	88	PMU: CHARGER BUCK	N/A	N/A
66	89	POWER: BATTERY CONN	N/A	N/A
67	90	SOC: DEBUG	N/A	N/A
68	91	ALIASES: BB/WLAN/BT	N/A	N/A
69	93	TEST: TPS/HOLES/FIDUCUALS	N/A	N/A
70	95	TEST: EE TP/PP	N/A	N/A
71	96	TEST: CELL EE TP/PP	N/A	N/A
72	121	POWER: ALIASES	N/A	N/A
73	155	BB/WLAN VOLTAGE ATTRIBUTES	N/A	N/A

DRAWING

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-0301	1	SCH,MLB-B,J82	SCH1	CRITICAL	
820-3638	1	PCBF,MLB-B,J82	PCB1	CRITICAL	

DRAWING TITLE: SCHEM,MLB-B,X190

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DRAWING NUMBER: 051-0301 SIZE: D

REVISION: B.0.0

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PAGE: 1 OF 155

SHEET: 1 OF 73

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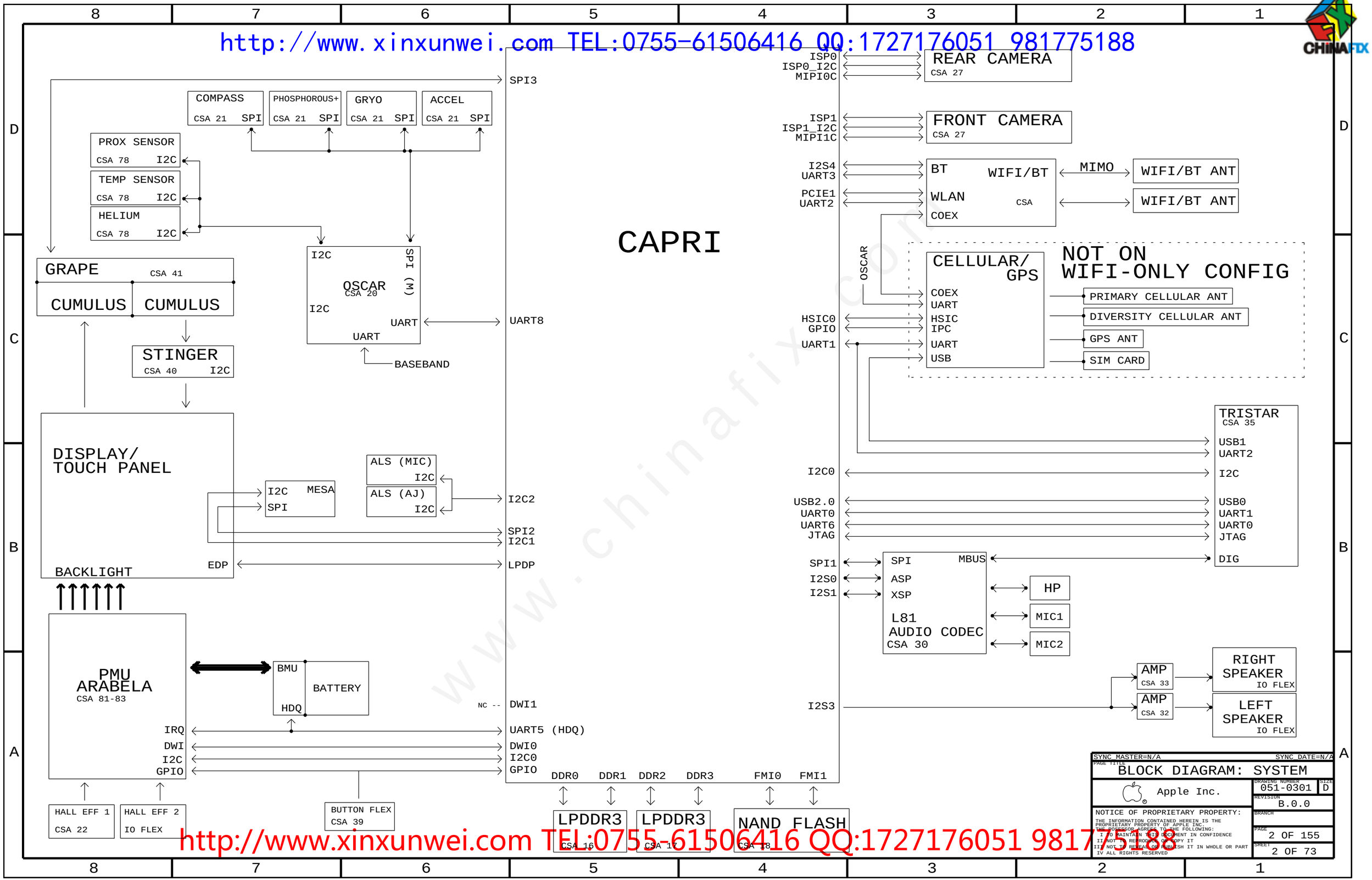

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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

SDC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S00016	1	IC,CAPRI,A1,PROD,ASE	U0600	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S00021	343S00016		U0600	IC,CAPRI,A1,PROD,SCK

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0675	1	IC,PMU,ARABELA,D2207A0,TOP-AC,FCBGA380	U8100	CRITICAL	

SDRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0803	2	IC,CAPRI,DRAM,10X10MM,FBGA261	U1600,U1700	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S0804	333S0803		U1600,U1700	ELPIDA DRAM
333S00014	333S0803		U1600,U1700	SAMSUNG DRAM

NAND

16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0972	1	TOSHIBA 16GB MLC 1YNM PPN1.5	U1800	CRITICAL	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S1035	335S0972	16GB_PROD	U1800	HYNIX 16GB MLC 1YNM PPN1.5

64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00011	1	SANDISK 64GB TLC 1YNM PPN1.5	U1800	CRITICAL	64GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00017	335S00011	64GB_PROD	U1800	TOSHIBA 64GB TLC 1YNM PPN

128GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00012	1	SANDISK 128GB TLC 1YNM PPN1.5	U1800	CRITICAL	128GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00018	335S00012	128GB_PROD	U1800	TOSHIBA 128GB TLC 1YNM PPN

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-7118	1	RADIO FENCE X190	PD_FENCE_RADIO	CRITICAL	MLB_B
806-00001	1	AP FENCE X190	PD_FENCE_AP	CRITICAL	
806-6353	1	GRAPE FENCE X190	PD_FENCE_GRAPE	CRITICAL	

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-00067	1	EEEE FOR 639-5813 (MLB A 16GB)	EEEE_FQJ3	CRITICAL	EEEE_MLB_A_16GB
825-00067	1	EEEE FOR 639-5814 (MLB A 32GB)	EEEE_FQJ0	CRITICAL	EEEE_MLB_A_32GB
825-00067	1	EEEE FOR 639-5815 (MLB A 64GB)	EEEE_FQJ1	CRITICAL	EEEE_MLB_A_64GB
825-00067	1	EEEE FOR 639-5816 (MLB A 128GB)	EEEE_FQJ2	CRITICAL	EEEE_MLB_A_128GB
825-00067	1	EEEE FOR 639-4747 (MLB B 16GB)	EEEE_FH54	CRITICAL	EEEE_MLB_B_16GB
825-00067	1	EEEE FOR 639-5809 (MLB B 32GB)	EEEE_FQHY	CRITICAL	EEEE_MLB_B_32GB
825-00067	1	EEEE FOR 639-5810 (MLB B 64GB)	EEEE_FQHW	CRITICAL	EEEE_MLB_B_64GB
825-00067	1	EEEE FOR 639-5811 (MLB B 128GB)	EEEE_FQHV	CRITICAL	EEEE_MLB_B_128GB

CKPLUS WAIVE TABLE

CKPLUS RULE EXCEPTIONS	REQUIRED
SCHEMATIC DEFINED CONSTRAINTS (YES/NO)	NO

SYNC MASTER=N/A SYNC DATE=N/A

PAGE TITLE
BOM TABLES

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PAGE 4 OF 155
SHEET 3 OF 73

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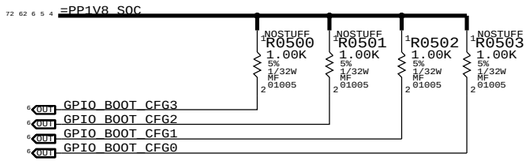
BOOT CONFIG ID

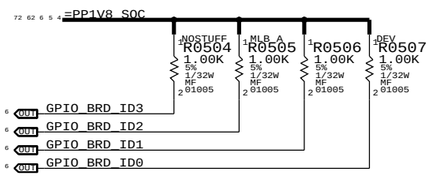


BOOT_CFG[3:0]	MODE
0000	SPI
0001	SPI W/TEST
CURRENT SETTING ---> 0010	NAND
0011	NAND W/TEST

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD ID

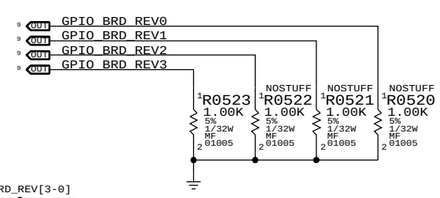


BRD_ID[3-0]	
0000	RESERVED
0001	RESERVED
0010	MLB_B AP
0011	MLB_B DEV (RDAR://PROBLEM/15529479)
0100	RESERVED
0101	RESERVED
0110	MLB_A AP
0111	MLB_A DEV (RDAR://PROBLEM/15529479)
1000	UNUSED
1001	UNUSED
1010	UNUSED
1011	UNUSED
1100	RESERVED
1101	RESERVED

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

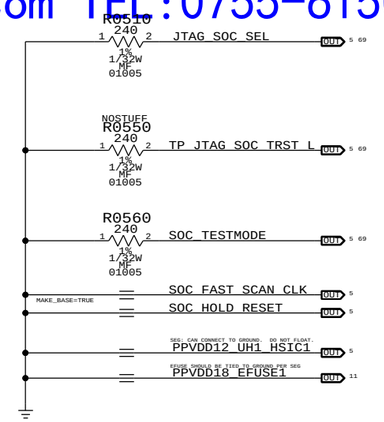
BOARD REVISION

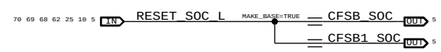


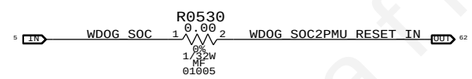
BRD_REV[3-0]	
0000	RESERVED
0001	RESERVED
0010	PROTO 1 (BRING UP)
0011	PROTO 1 (LOCAL/CHINA)
0100	PROTO 2
0101	PRE-EVT
0110	EVT
CURRENT SETTING ---> 0111	DVT & PVT
1000	UNUSED

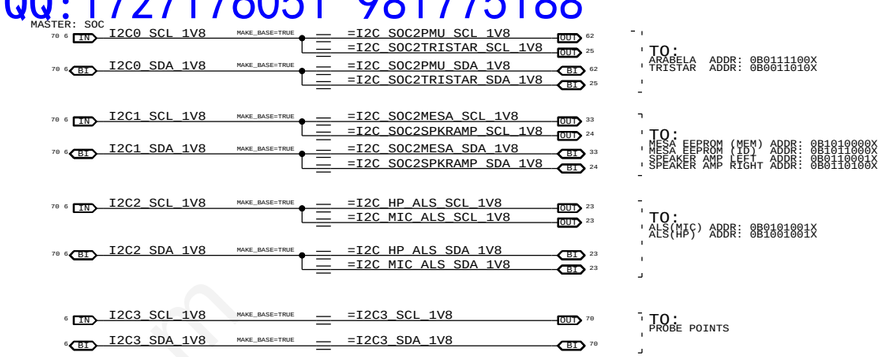
S/W READ FLOW

1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ









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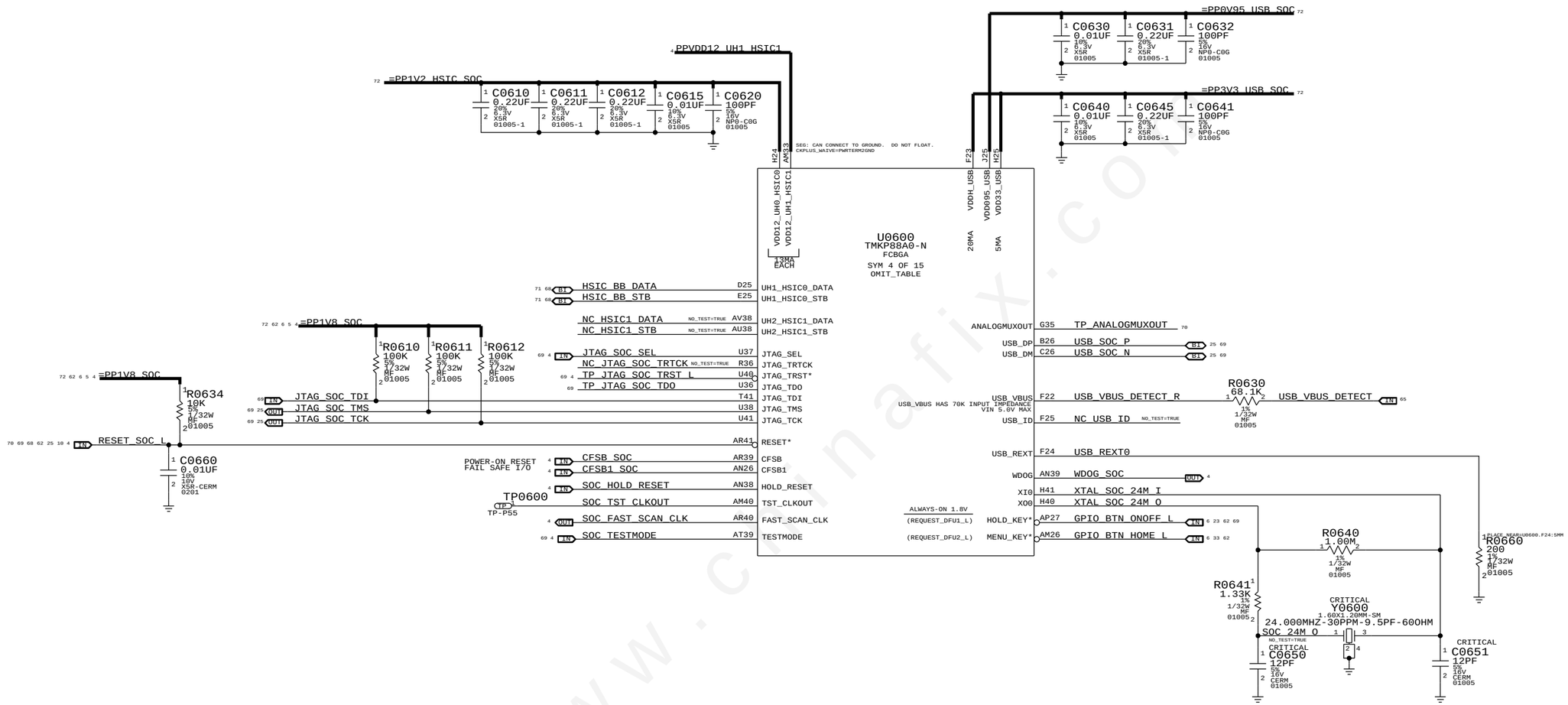
ON IN HIBERNATE
VDD1, VDD2, VDDIOD_DDRXCA (VDDCA), VDD12_CKE_DDR0, VDD12_CKE_DDR1



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PAGE TITLE
SOC: MAIN

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PAGE 6 OF 155
SHEET 5 OF 73

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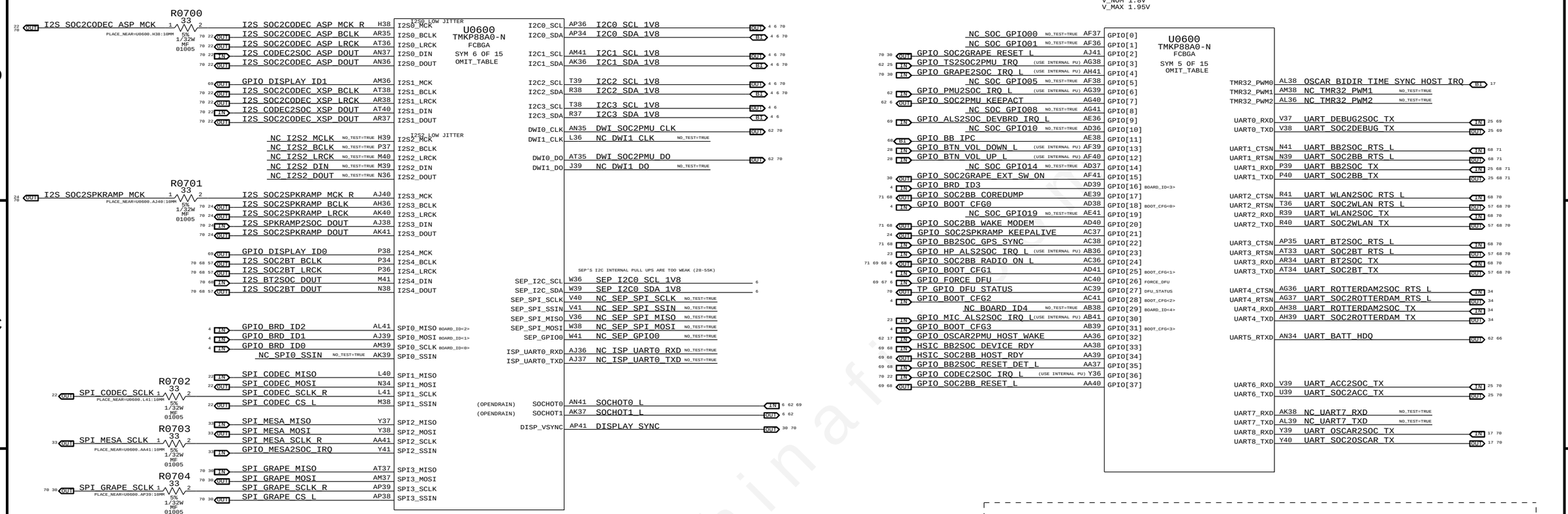

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PAGE TITLE: SOC: I/OS

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PAGE: 7 OF 155

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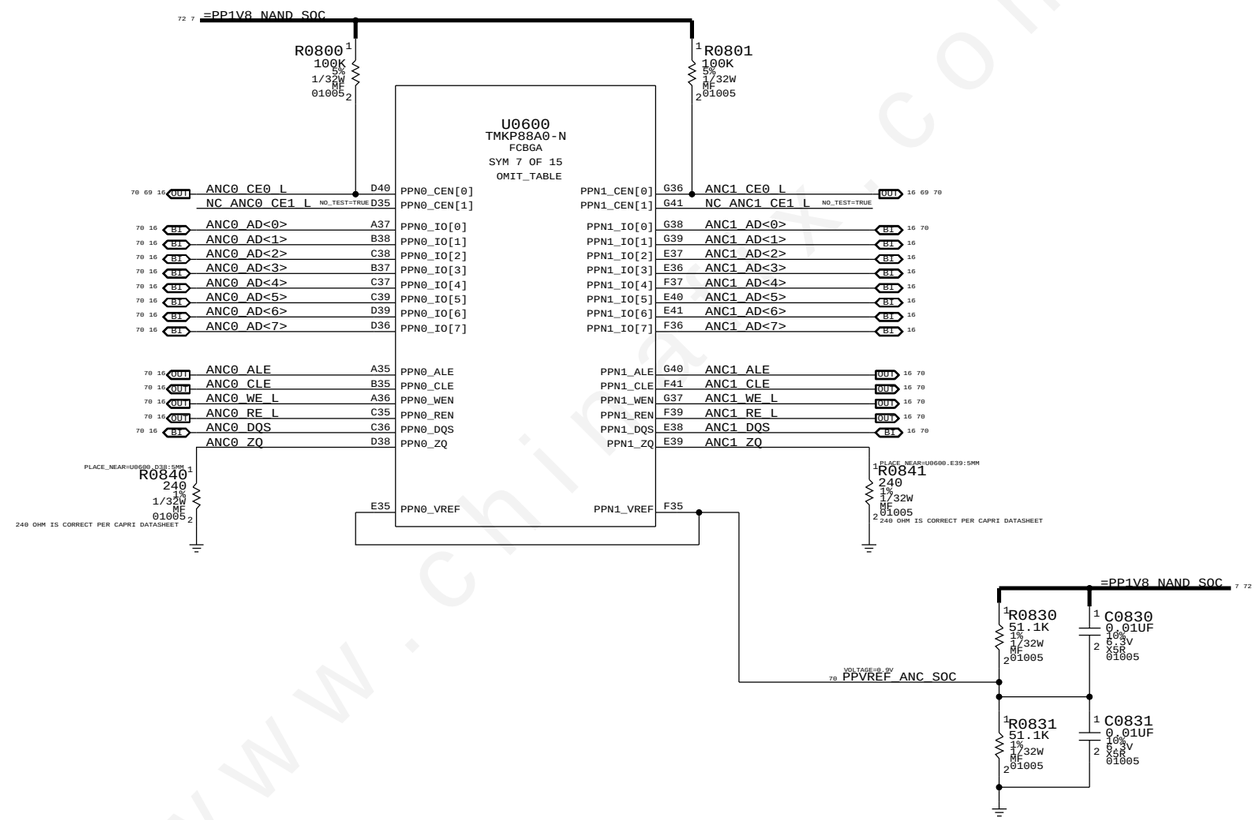

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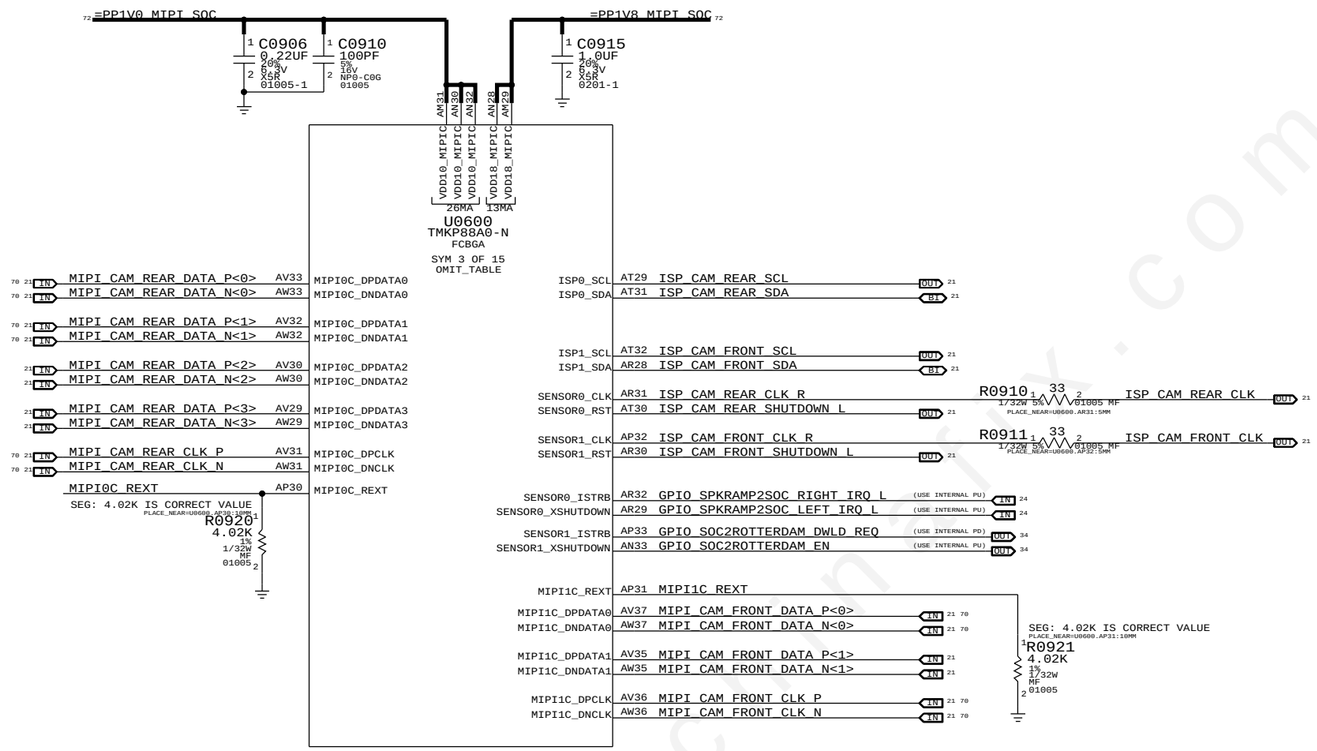

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	PAGE 9 OF 155
	SHEET 8 OF 73

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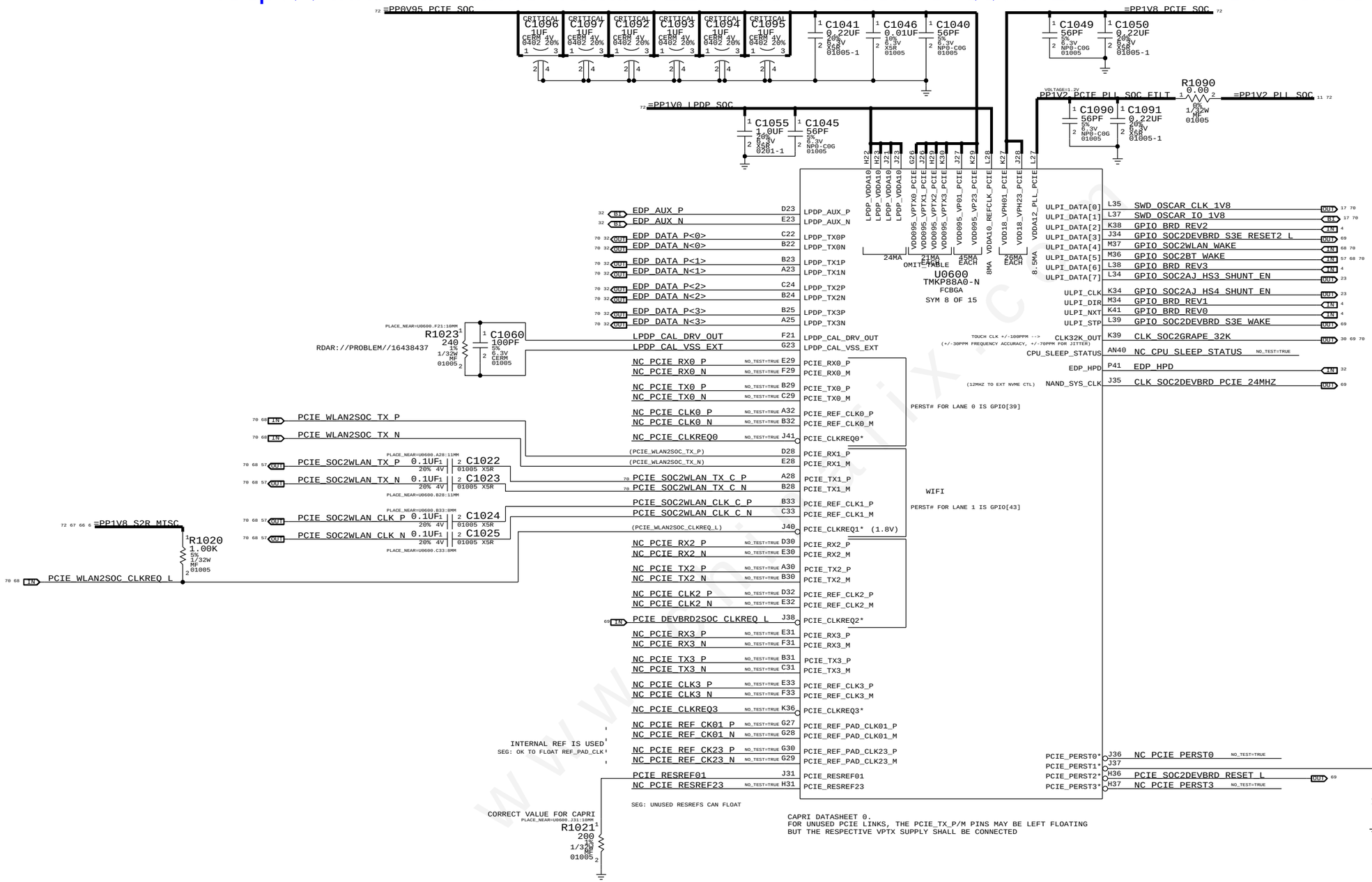

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SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: SOC: EDP, PCIE

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PAGE: 10 OF 155

SHEET: 9 OF 73

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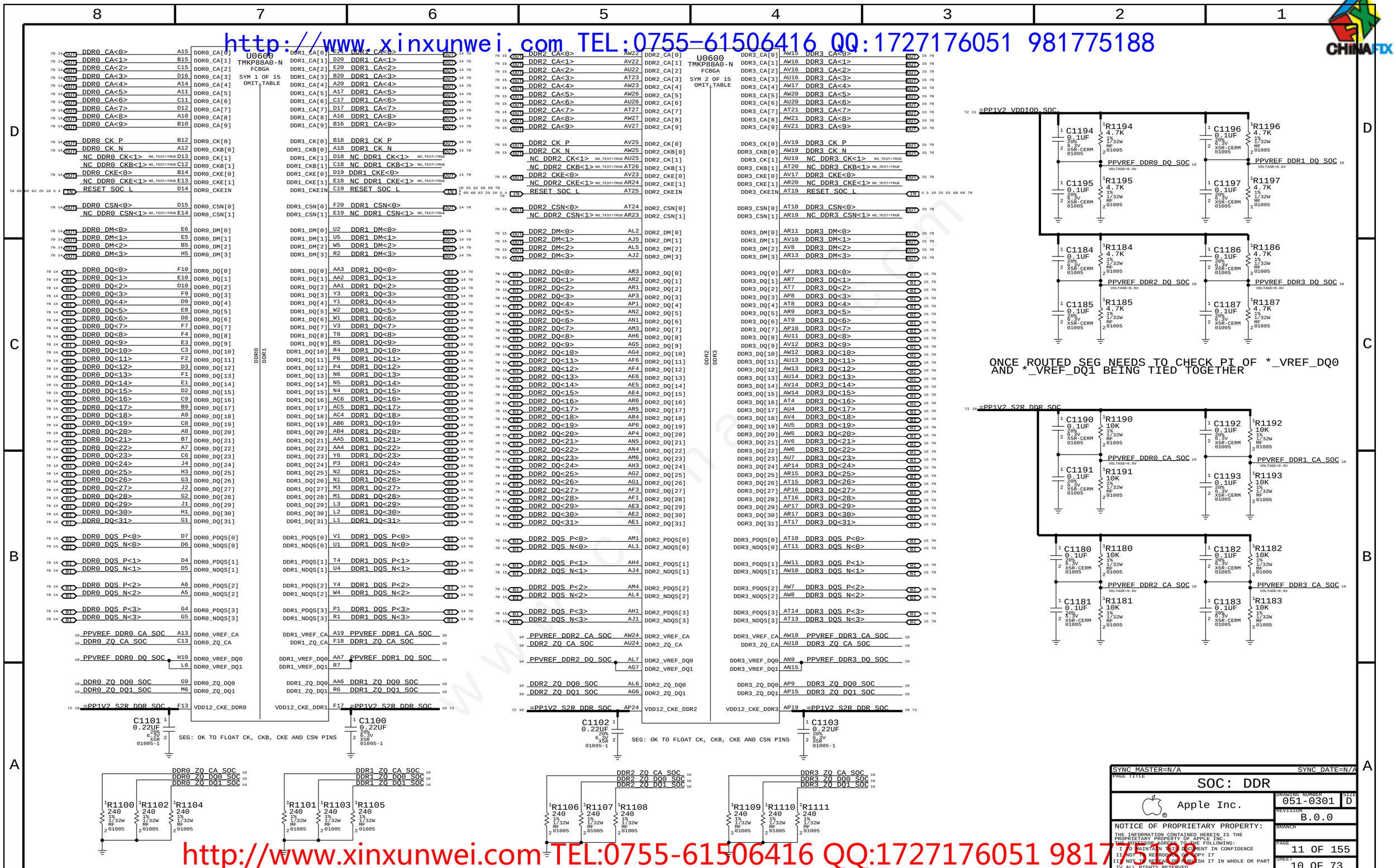

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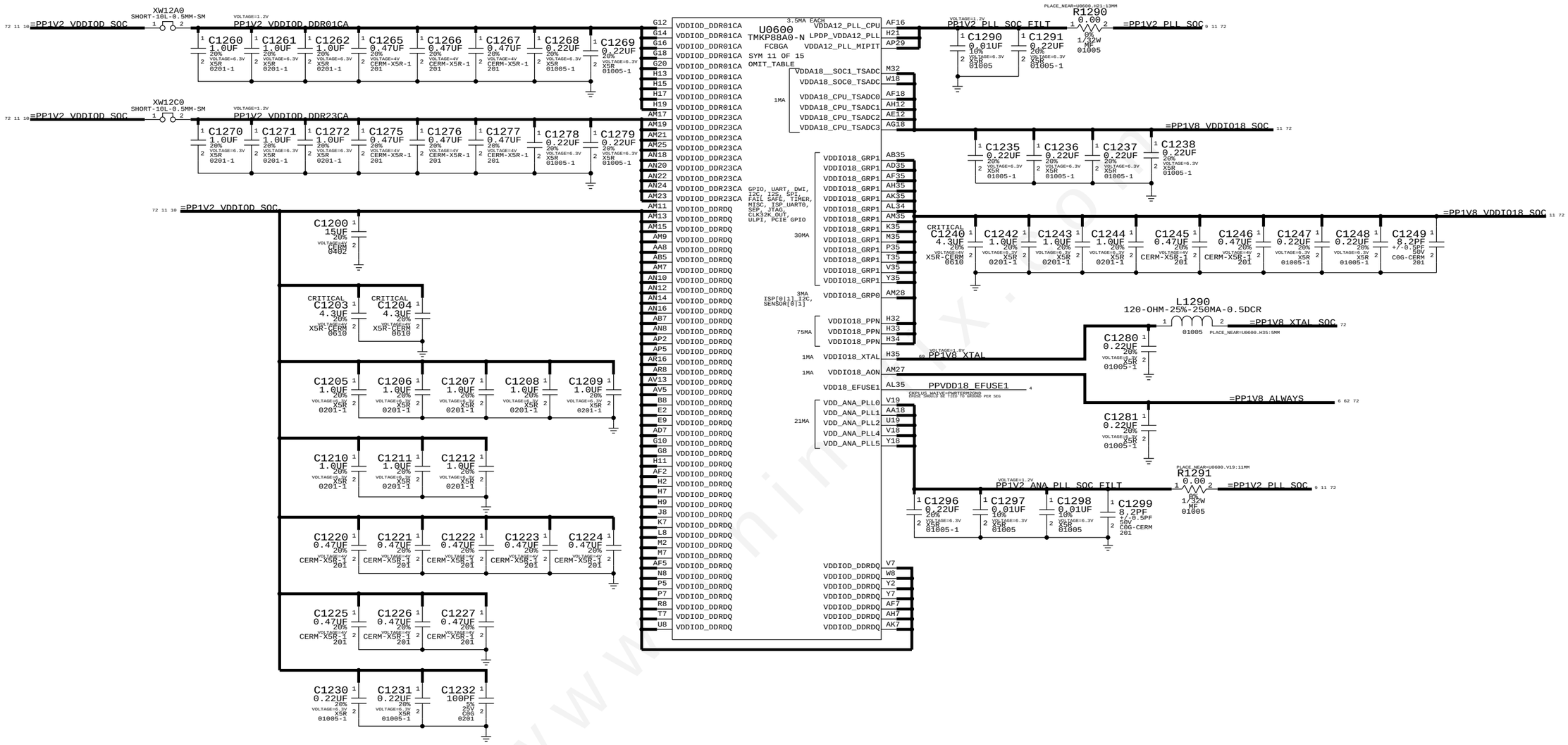

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138S0702	138S0657			QTY 22 RDAR://PROBLEM/8837828

REFDES FOR ALTERATIVE TABLE

C1203,C1204,C1240, C1305-C1308, C1404-C1409,C1464-C1469,C1445,C1446

C1602,C1603,C1642,C1643, C1702,C1703,C1742,C1743

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: SOC: IO POWER

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DRAWING NUMBER: 051-0301 SIZE: D

REVISION: B.0.0

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PAGE: 12 OF 155

SHEET: 11 OF 73

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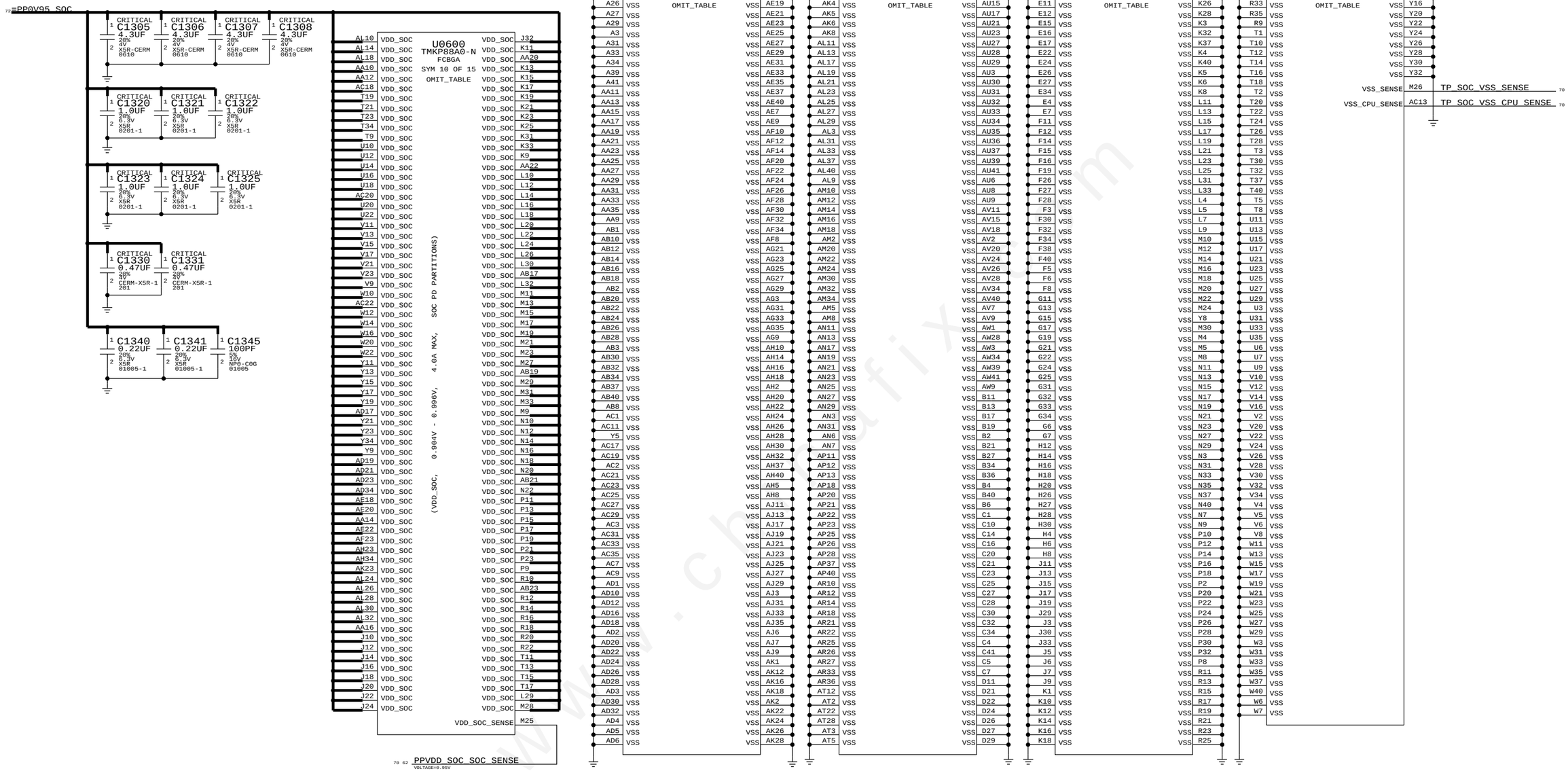

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SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
SOC: SOC POWER AND GND

Apple Inc.

DRAWING NUMBER 051-0301 SIZE D

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PAGE 13 OF 155

SHEET 12 OF 73

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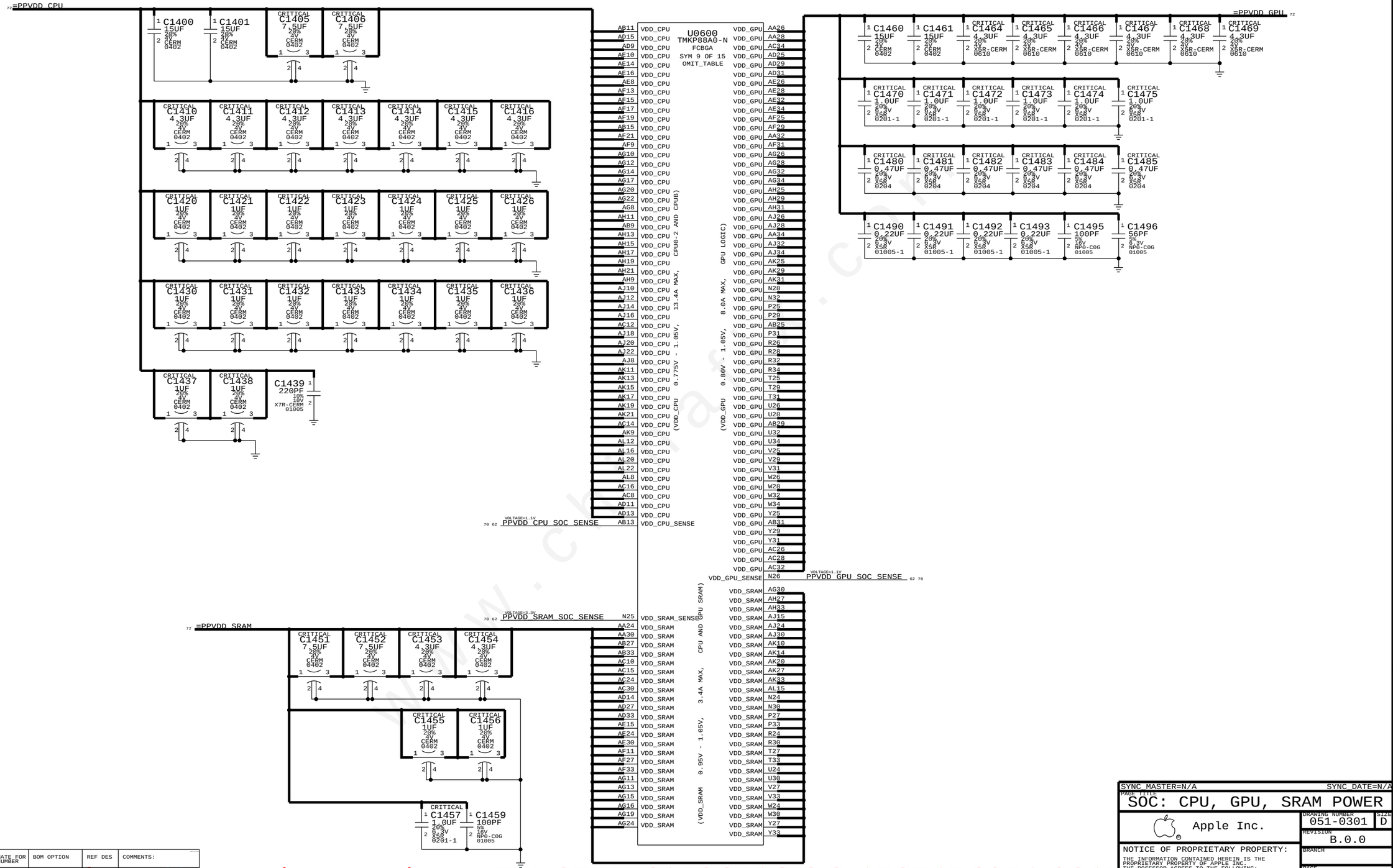

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SYNC MASTER=N/A SYNC DATE=N/A

PAGE TITLE
SOC: CPU, GPU, SRAM POWER

Apple Inc.

DRAWING NUMBER 051-0301 SIZE D

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PAGE 14 OF 155

SHEET 13 OF 73

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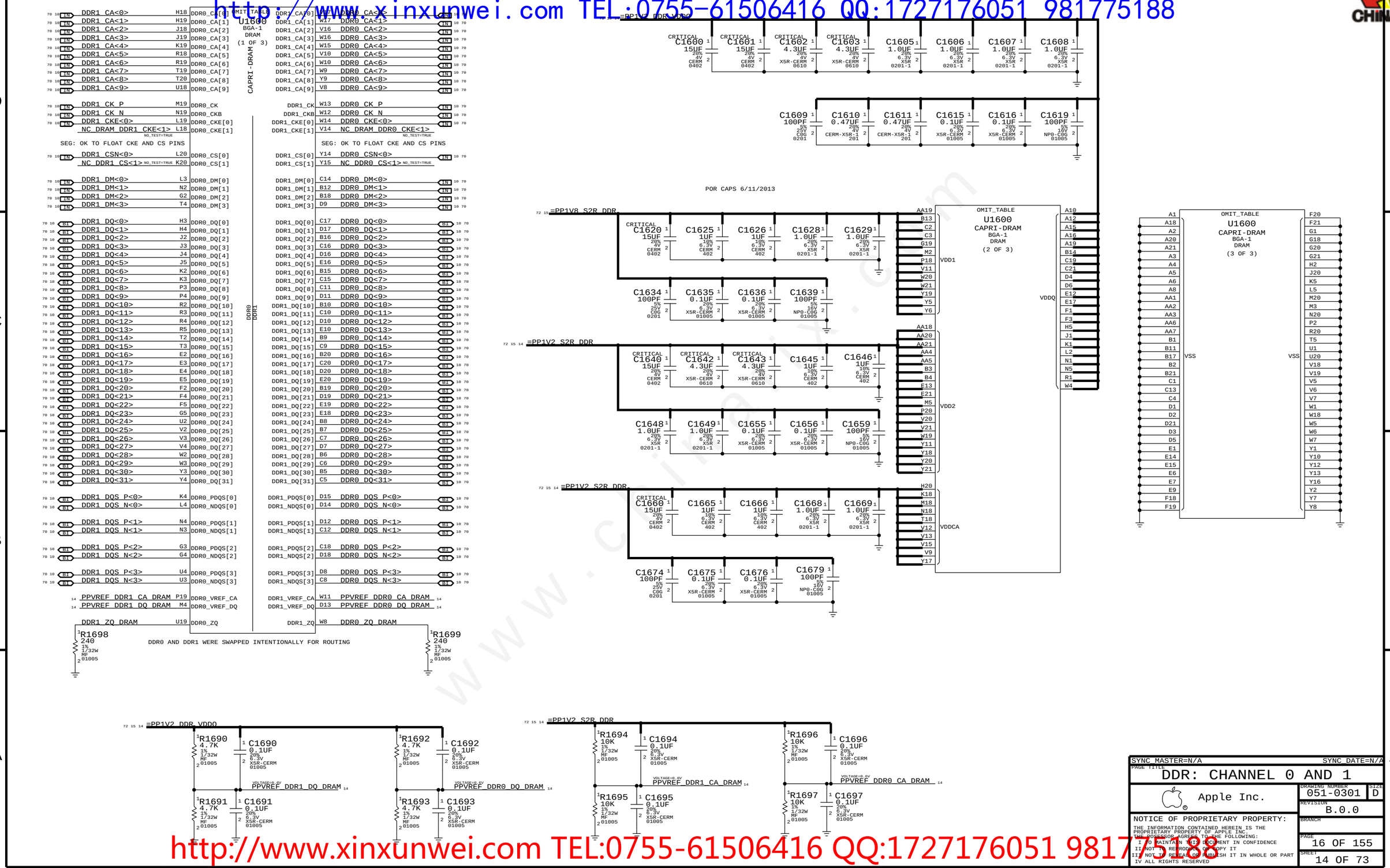

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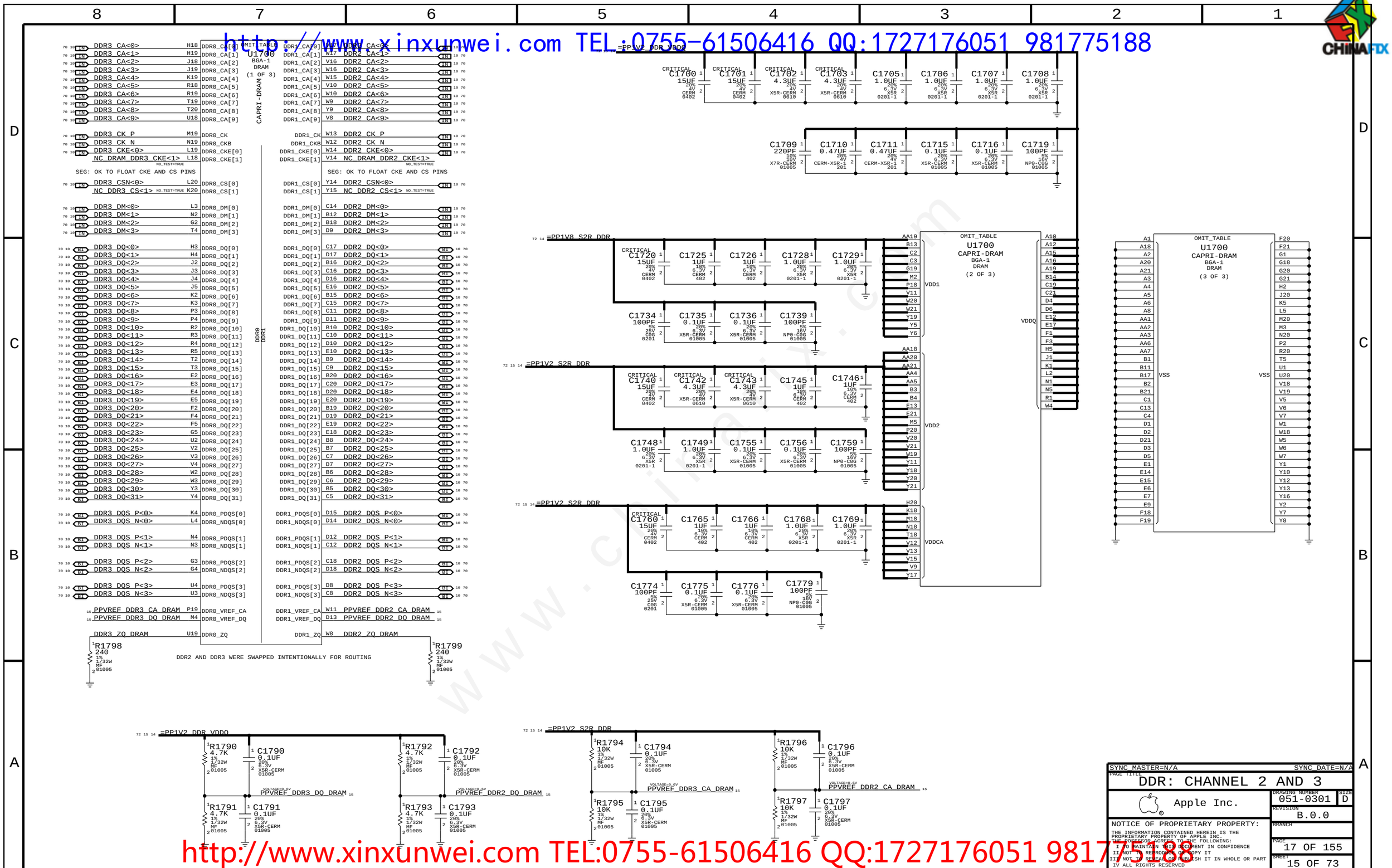

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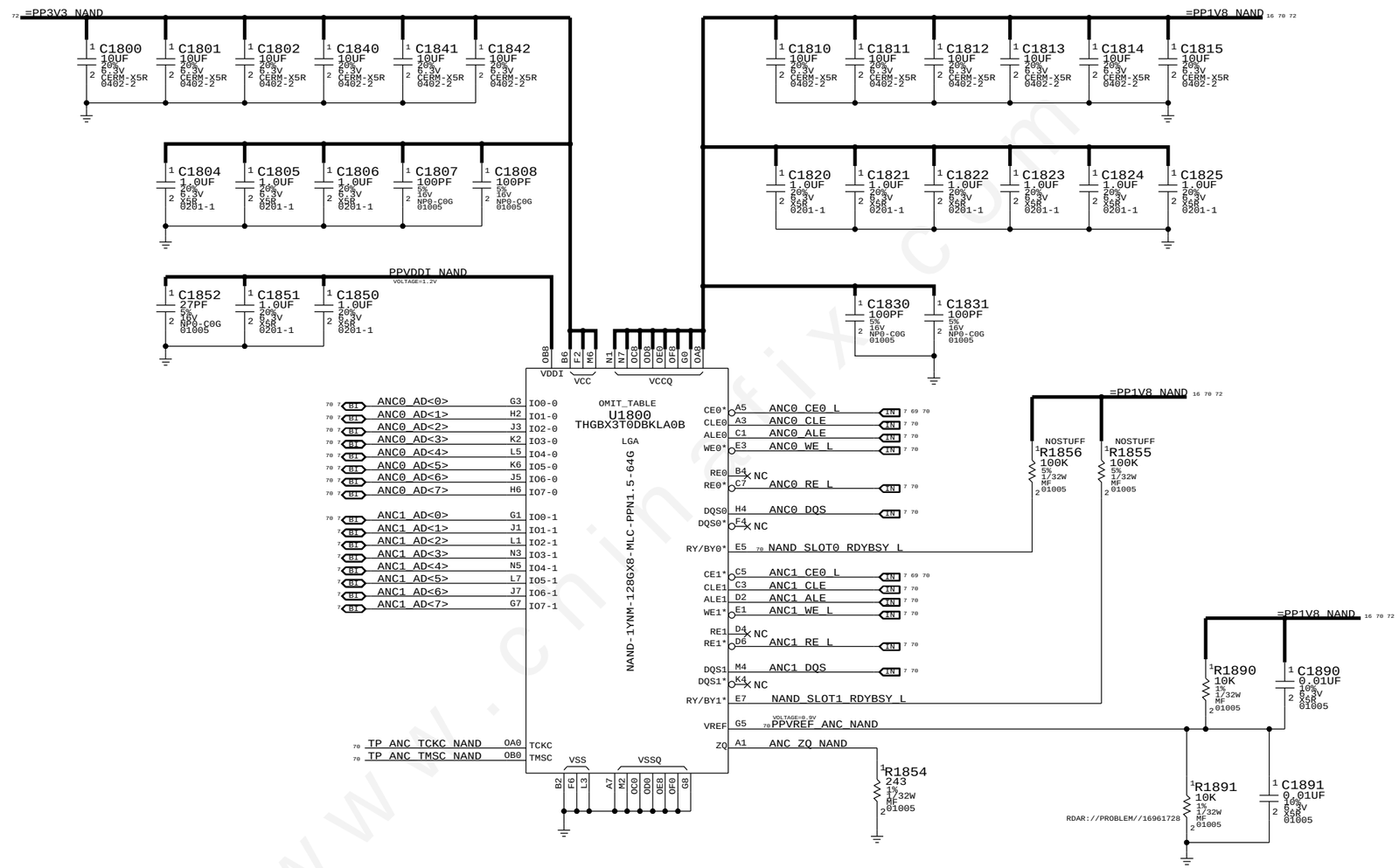

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DRAWING NUMBER: 051-0301 SIZE: D

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PAGE: 18 OF 155

SHEET: 16 OF 73

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OSCAR

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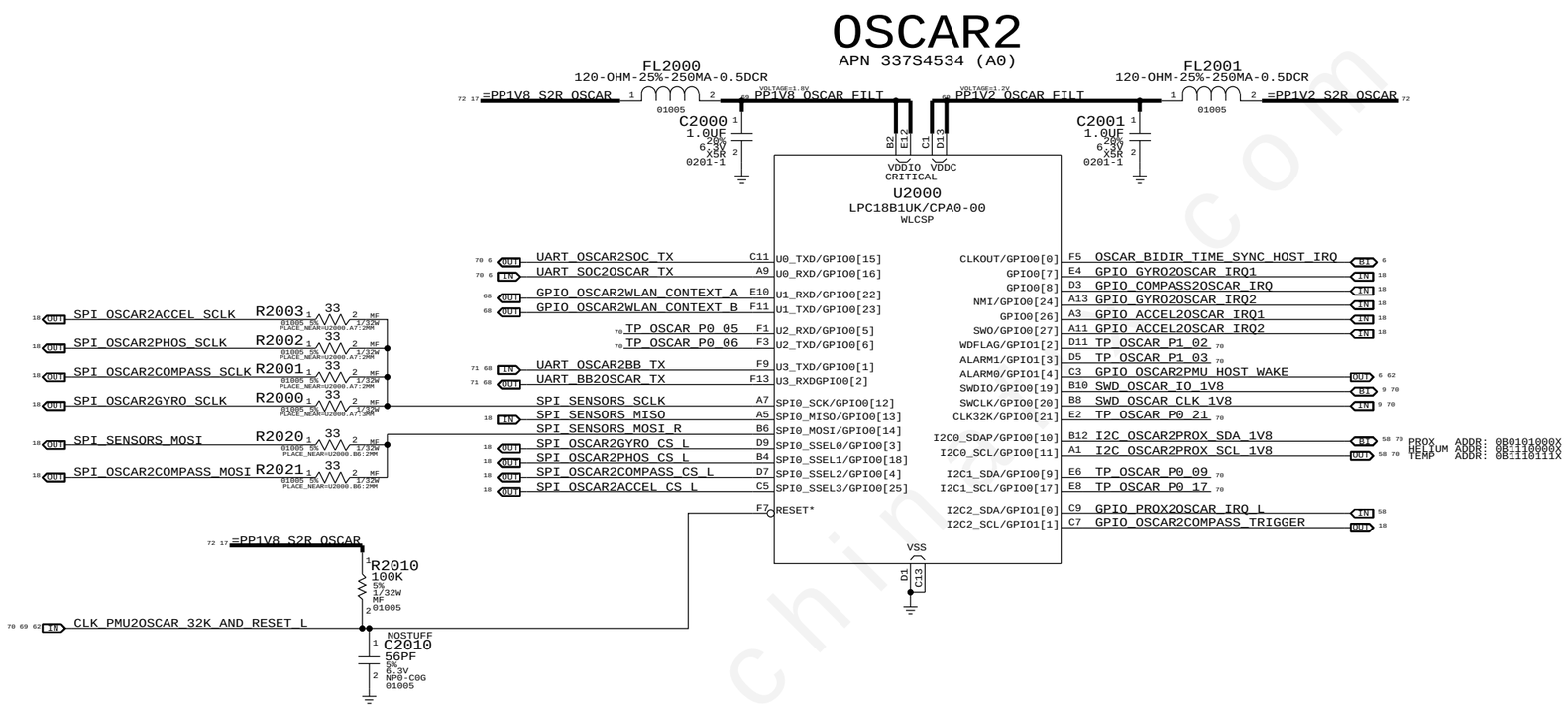

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SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
SENSOR: OSCAR

Apple Inc.

DRAWING NUMBER 051-0301 SIZE D
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BRANCH
PAGE 20 OF 155
SHEET 17 OF 73

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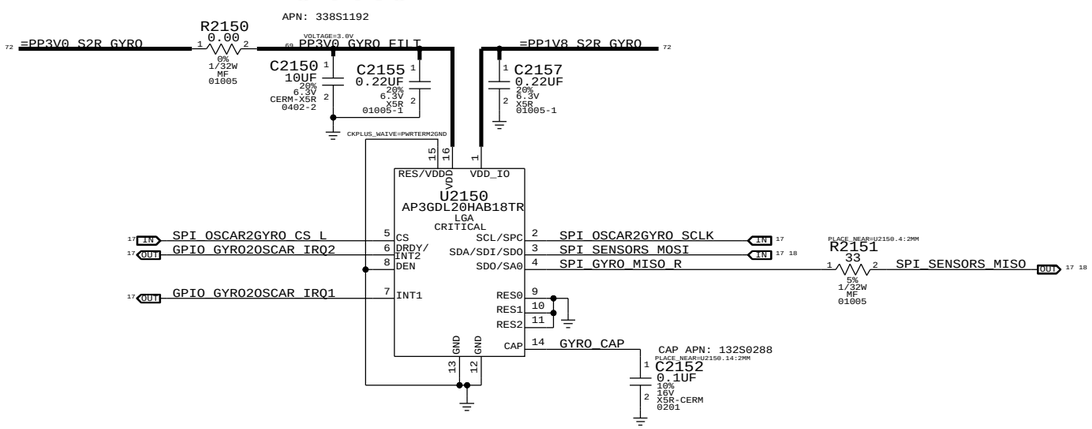
SENSORS

GYRO



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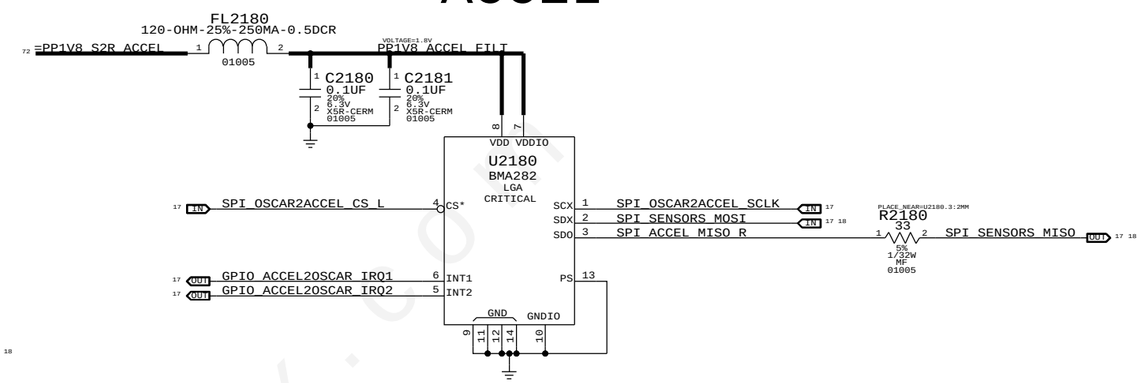
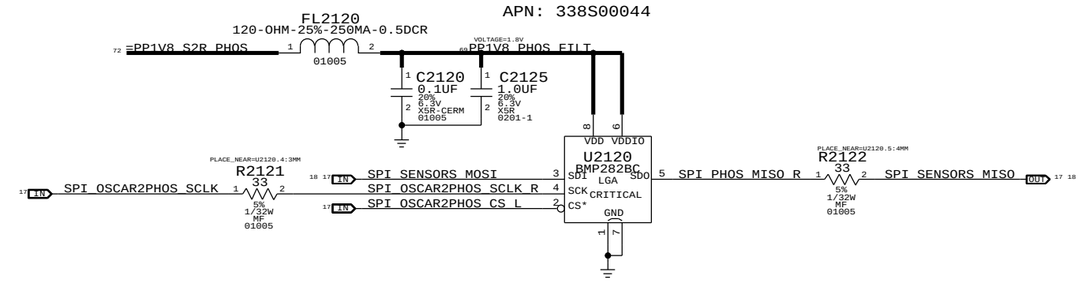


PHOSPHORUS

APN: 338S00044



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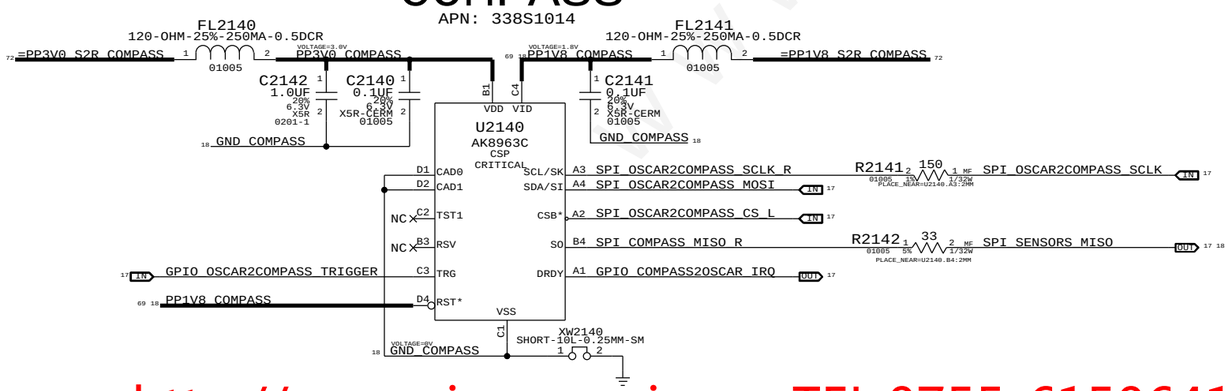

SYNC_MASTER=N/A	SYNC_DATE=N/A
PAGE TITLE: SENSOR: CARBON, PHOS+, MAGN	
Apple Inc.	DRAWING NUMBER 051-0301 SIZE D
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	PAGE 21 OF 155
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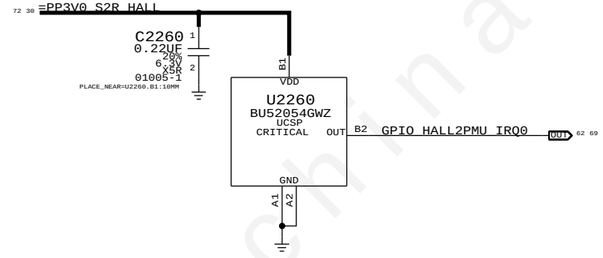
HALL EFFECT

HALL EFFECT

APN 353S3687



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SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
SENSOR: HALL EFFECT

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PAGE 22 OF 155

SHEET 19 OF 73

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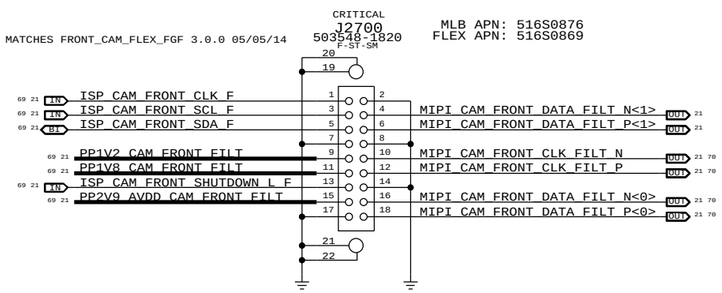
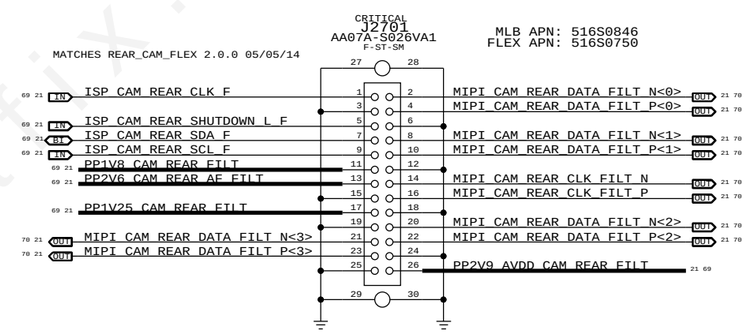
FRONT & REAR CAMERA CONNECTORS

FRONT CAMERA CONNECTOR



REAR CAMERA CONNECTOR



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PAGE TITLE: CAMERA: CAM CONNS

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DRAWING NUMBER: 051-0301 SIZE: D

REVISION: B.0.0

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PAGE: 27 OF 155

SHEET: 20 OF 73

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S00184	7	FERRITE,90OHM@25%,500MA,0.18OHM	FL2800,FL2802,FL2803,FL2861,FL2871,FL2881,FL2891	CRITICAL	
155S0667	8	COMMON MODE CHOKE,90OHM,100MA	L2810,L2811,L2812,L2852,L2853,L2854,L2855,L2856	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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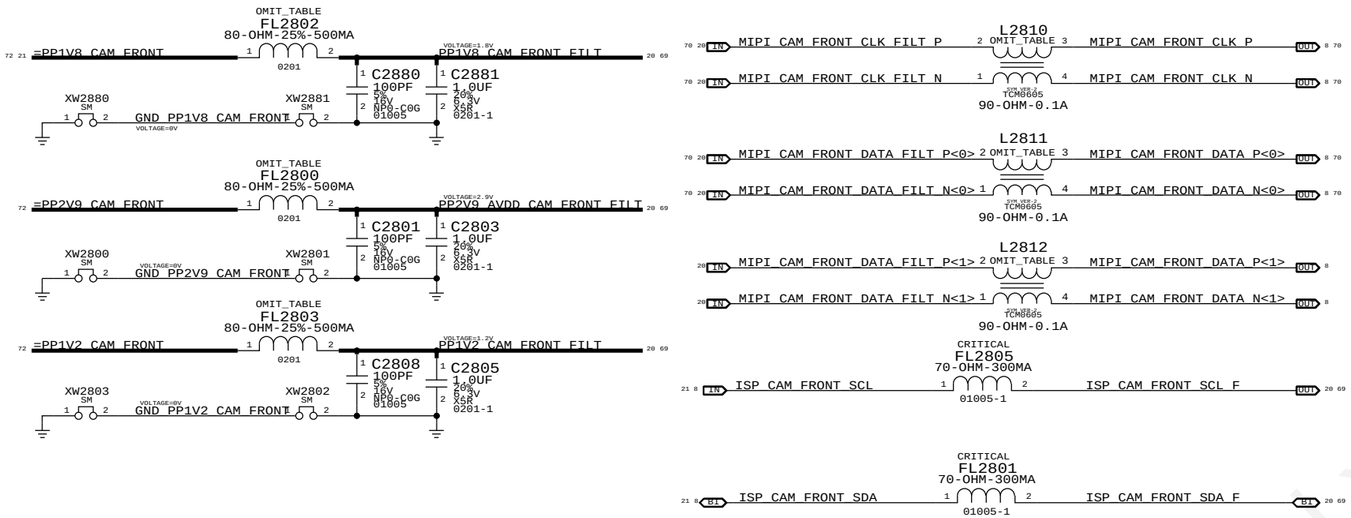
FRONT CAMERA SUPPORT



REAR CAMERA SUPPORT

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PAGE TITLE
CAMERA: CAM SUPPORT

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PAGE 28 OF 155

SHEET 21 OF 73

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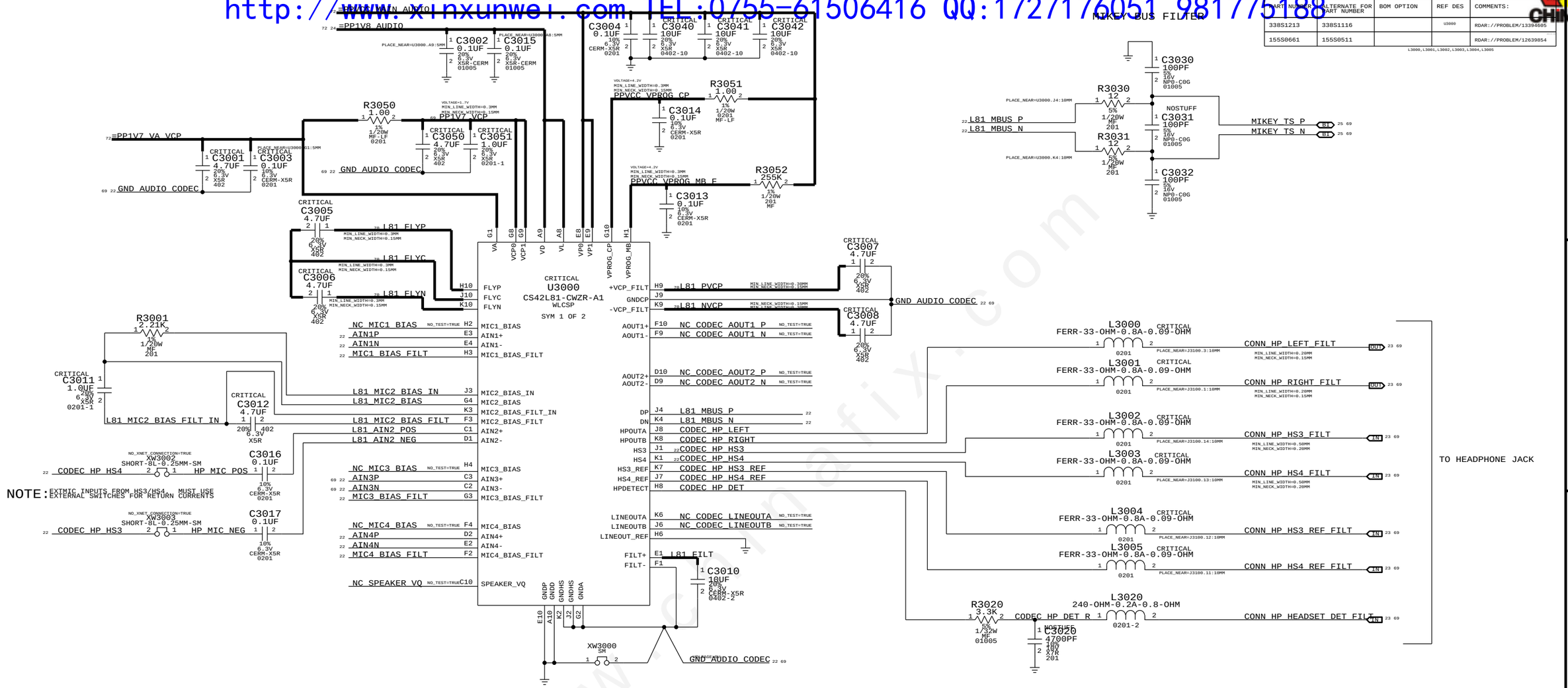
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S1213	338S1116		U3000	RDAR://PROBLEM/13394605
155S0661	155S0511			RDAR://PROBLEM/12639854

L3000,L3001,L3002,L3003,L3004,L3005



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PAGE TITLE: AUDIO: L81 CODEC

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DRAWING NUMBER: 051-0301 SIZE: D

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PAGE: 30 OF 155

SHEET: 22 OF 73

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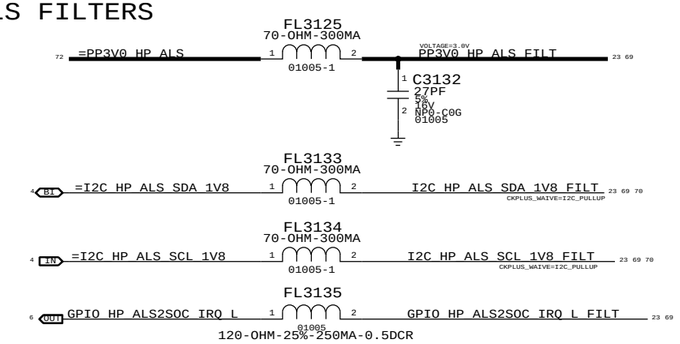
AUDIO JACK AND DMIC CONN

ALS FILTERS



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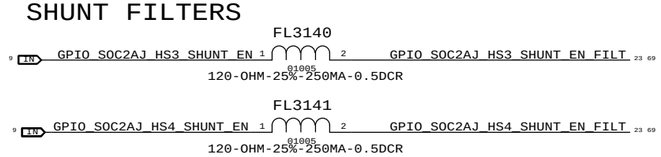

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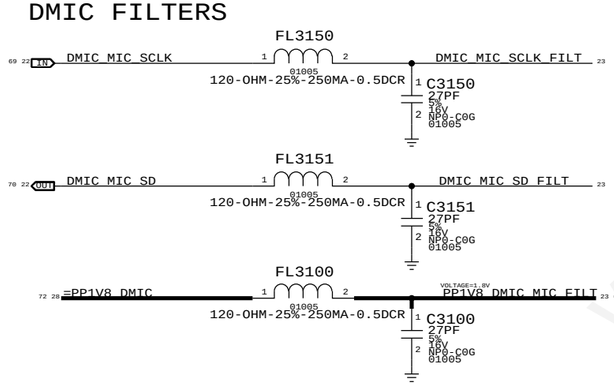
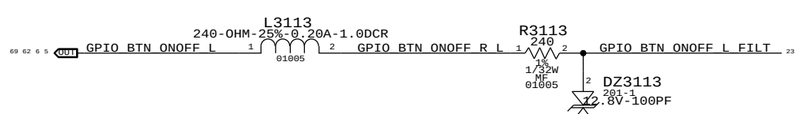
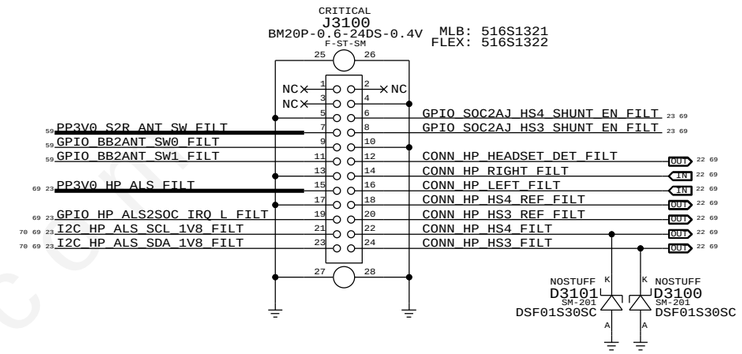




AUDIO JACK B2B CONNECTOR

MATCHES ALS_AUDIO_JACK_FLEX 2.1.0 02/18/14



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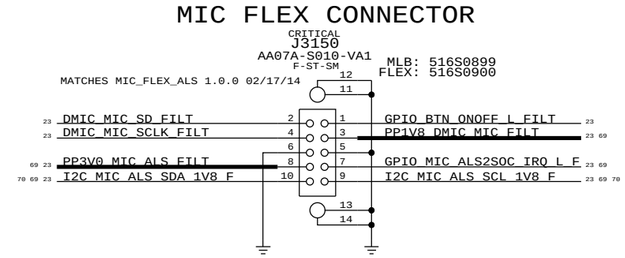

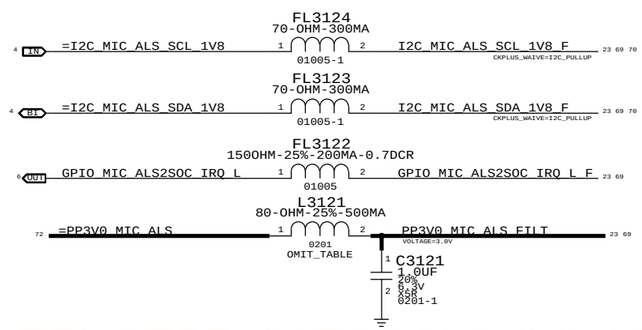

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
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SYNC MASTER=N/A SYNC DATE=N/A

PAGE TITLE
AUDIO: HP/DMIC FLEX CONNS

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PAGE 31 OF 155

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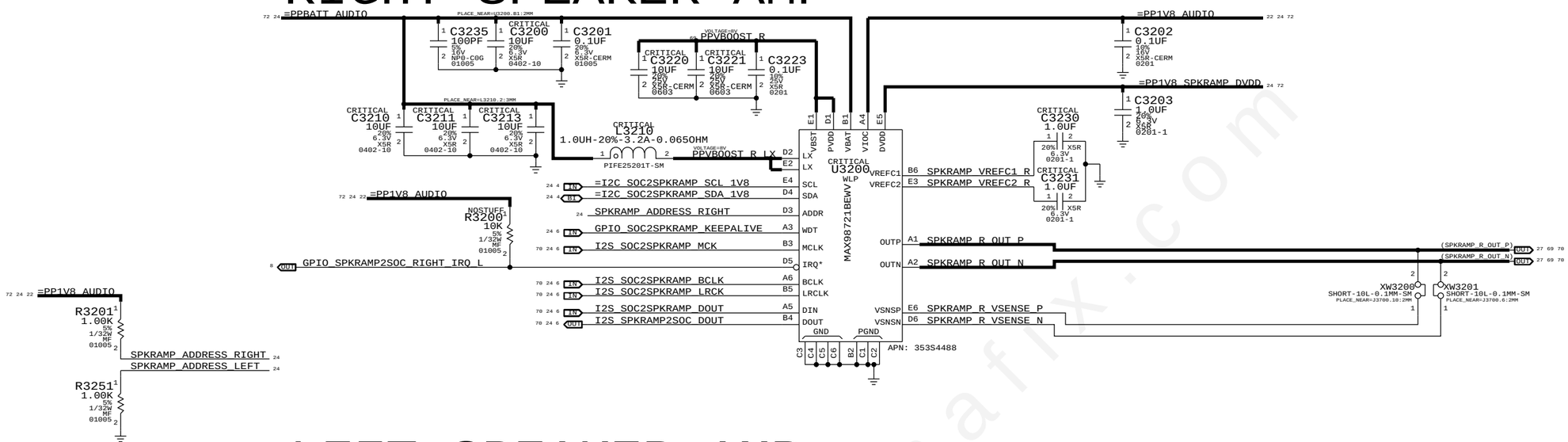
RIGHT SPEAKER AMP



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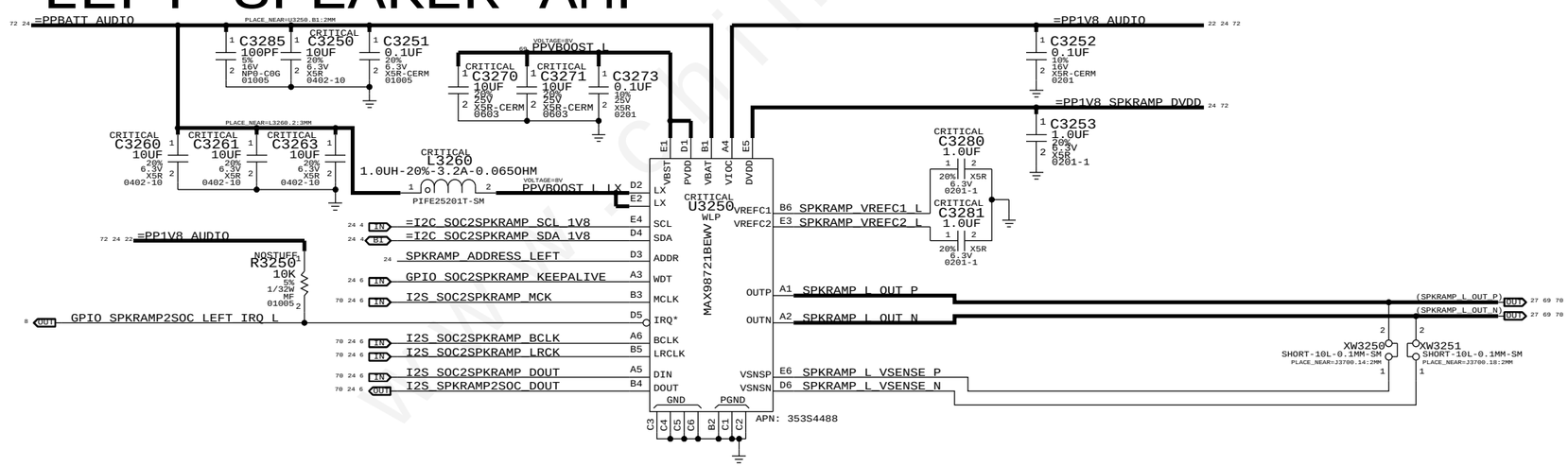

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PAGE TITLE: AUDIO: SPEAKER AMPS	
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	PAGE 32 OF 155
	SHEET 24 OF 73

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0667	2	COMMON MODE CHOKE,90OHM,100MA	L3530,L3531	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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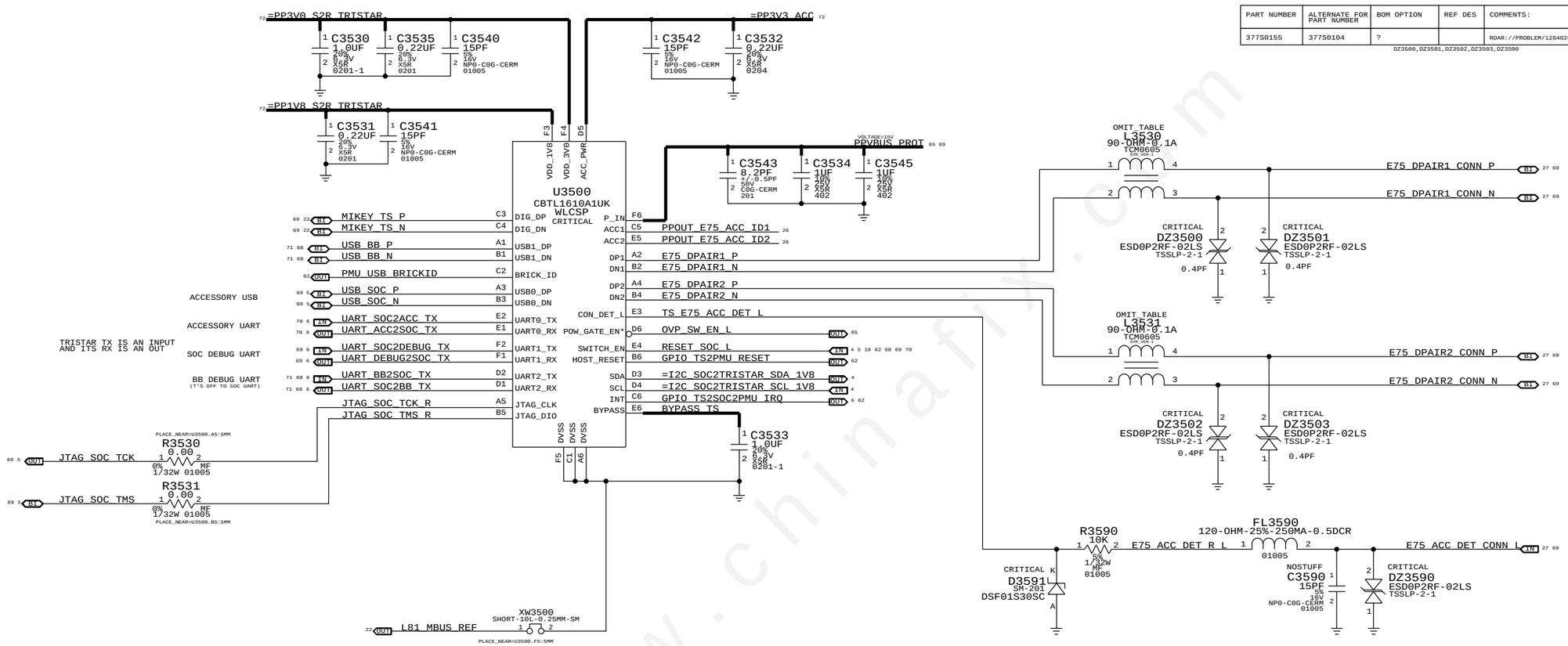

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: IO: TRISTAR

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BRANCH:

PAGE: 35 OF 155

SHEET: 25 OF 73

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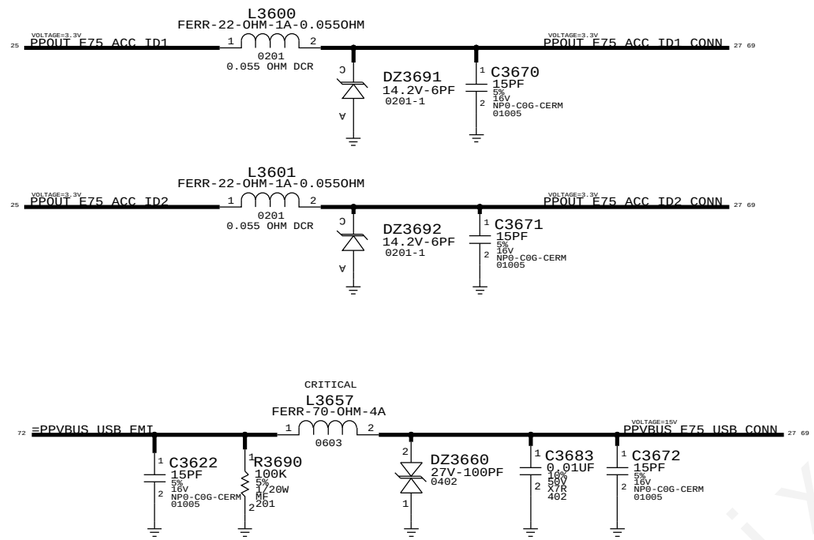

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155S0741	155S0397		L3657	RDAR://PROBLEM/11238851

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SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
IO: FILTERS

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REVISION B.0.0
BRANCH
PAGE 36 OF 155
SHEET 26 OF 73

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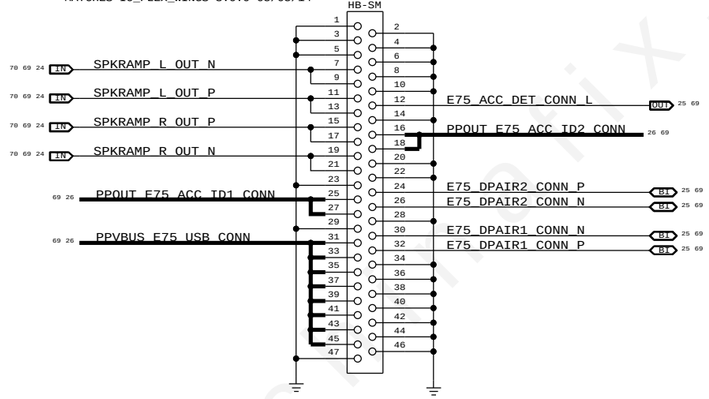
IO FLEX HOTBAR PADS

MATCHES IO_FLEX_WINGS 3.0.0 05/05/14

OMIT
J3700
PCB-X110
HB-SM

MLB: 998-5877
FLEX: 998-5876



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PAGE TITLE
IO: HOTBAR PADS

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DRAWING NUMBER 051-0301 SIZE D
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PAGE 37 OF 155
SHEET 27 OF 73

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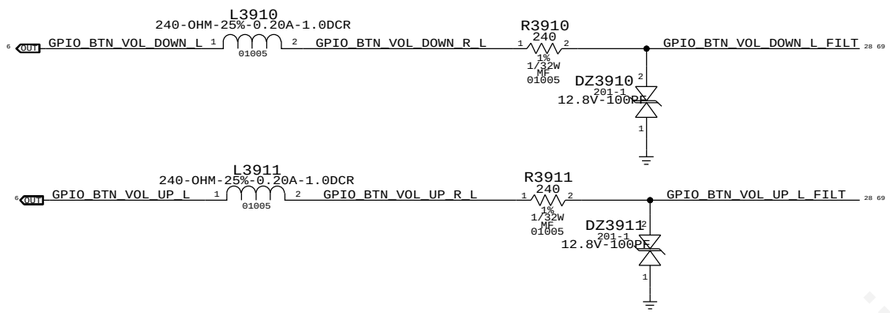
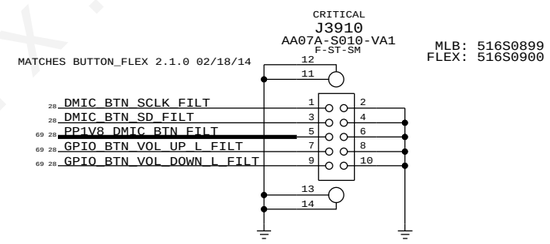
BUTTON CONNECTOR





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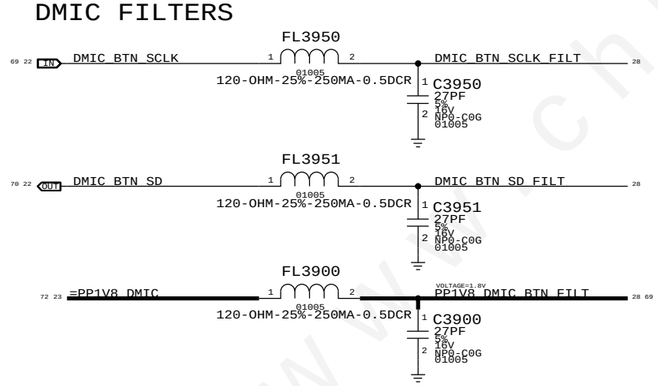

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	SHEET 28 OF 73

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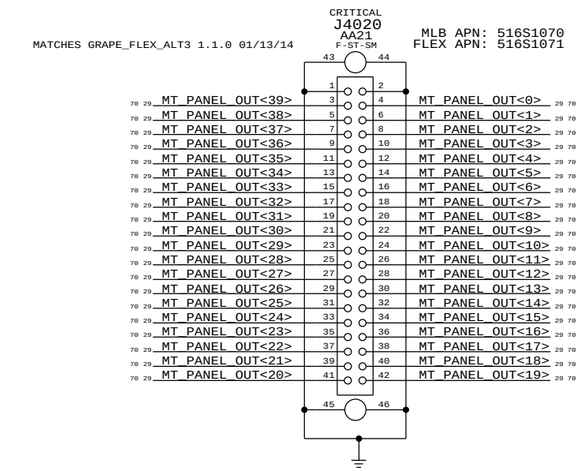
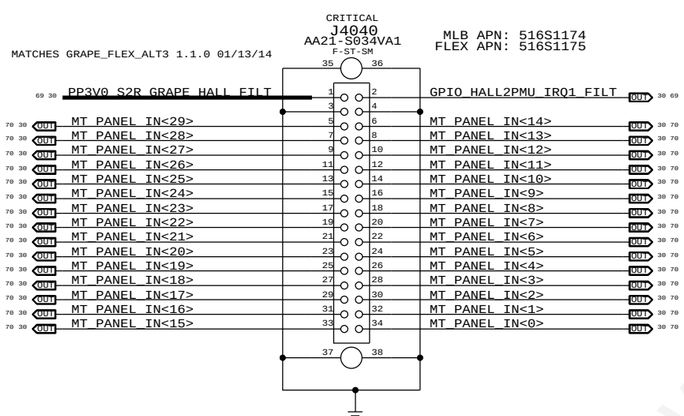
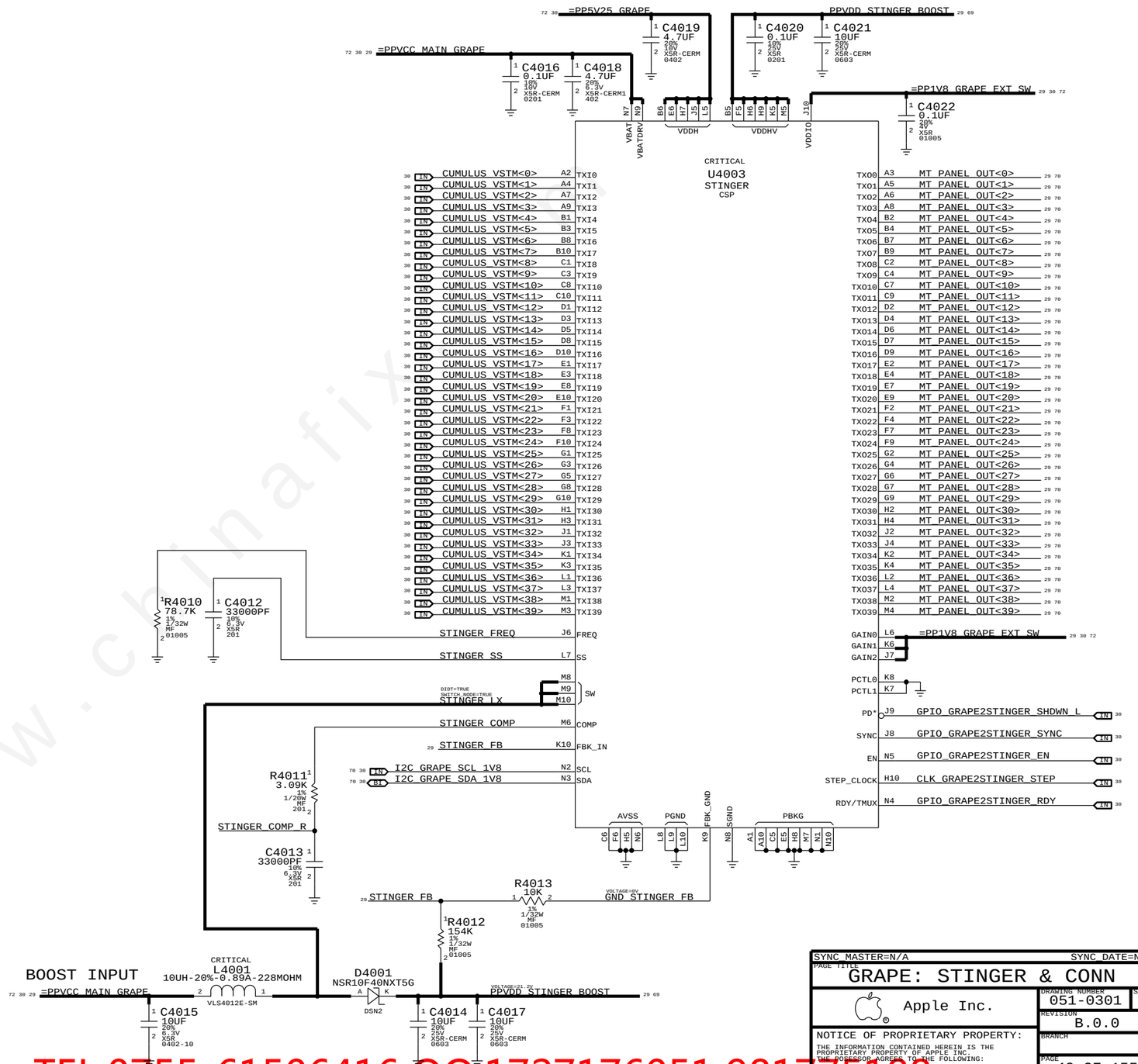
STINGER







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GRAPE: STINGER & CONN

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BRANCH
PAGE 40 OF 155
SHEET 29 OF 73

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S00018	2	IC,CUMULUS,C1,OPTION1	U4100,U4150	CRITICAL	

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=PP1V8_GRAPE_EXT_SW
R4102 4.7K 1% 1/32W MF 01005 — CUMULUS_M_BCFG_RTCK
R4104 4.7K 1% 1/32W MF 01005 — JTAG_CUMULUS_M_TMS
R4152 4.7K 1% 1/32W MF 01005 — JTAG_CUMULUS_S_TMS
R4154 4.7K 1% 1/32W MF 01005 — CUMULUS_S_BCFG_RTCK

=PP1V8_GRAPE_EXT_SW
R4180 4.7K 1% 1/32W MF 01005 — I2C_GRAPE_SCL_1V8
R4181 4.7K 1% 1/32W MF 01005 — I2C_GRAPE_SDA_1V8

MASTER CUMULUS

=PP5V25_GRAPE
C4100 1UF 20% 10V X5R 0201
C4101 100PF 5% 16V NP0-C0G 01005

=PP1V8_GRAPE_EXT_SW
C4106 0.1UF 20% 4V X5R 01005

PPVDDCORE_CUMULUS_M (VOLTAGE=1.8V)
C4105 56PF 5% 6.3V NP0-C0G 01005
C4102 2.2UF 20% 4V X5R-CERM 0201

PPVDDANA_CUMULUS_M (VOLTAGE=1.8V)
C4103 2.2UF 20% 4V X5R-CERM 0201
C4104 56PF 5% 6.3V NP0-C0G 01005

=PP1V8_GRAPE_EXT_SW
C4108 4.7UF 20% 6.3V X5R-CERM1 402
C4109 0.1UF 20% 4V X5R 01005
C4110 100PF 5% 6.3V CERM 01005

U4100 CUMULUS-C1 WLBGA OMIT_TABLE

Pin	Net	Pin	Net
B9	MT_PANEL_IN<0>	IN0_0	
B8	MT_PANEL_IN<1>	IN1_0	
A9	MT_PANEL_IN<2>	IN2_0	
B7	MT_PANEL_IN<3>	IN3_0	
B6	MT_PANEL_IN<4>	IN4_0	
A8	MT_PANEL_IN<5>	IN5_0	
B5	MT_PANEL_IN<6>	IN6_0	
B4	MT_PANEL_IN<7>	IN7_0	
A7	MT_PANEL_IN<8>	IN8_0	
B3	MT_PANEL_IN<9>	IN9_0	
A6	MT_PANEL_IN<10>	IN10_0	
A3	MT_PANEL_IN<11>	IN11_0	
A5	MT_PANEL_IN<12>	IN12_0	
A4	MT_PANEL_IN<13>	IN13_0	
B2	MT_PANEL_IN<14>	IN14_0	
A2	NC_CUMULUS_M_IN14_1 (NO_TEST=TRUE)	IN14_1	
E4	SPI_GRAPE_CS_L	H_CS*	
F1	GPIO_GRAPE2SOC_IRQ_L	H_INT*	
D3	SPI_GRAPE_SCLK	H_SCLK	
D2	SPI_GRAPE_MOSI	H_SDI	
E1	SPI_GRAPE_MISO	H_SDO	
C4	TP_JTAG_CUMULUS_M_TCK	JTAG_TCK	
C3	TP_JTAG_CUMULUS_M_TDI	JTAG_TDI	
E2	I2C_GRAPE_SDA_1V8	JTAG_TDO	
C6	JTAG_CUMULUS_M_TMS	JTAG_TMS	
E3	CUMULUS_M_BCFG_RTCK	BCFG_RTCK	
D1	CLK_SOC2GRAPE_32K	CLKIN/RESET*	
D9		RSTOVR*	
VSTM_0	CUMULUS_VSTM<0>		
E9	CUMULUS_VSTM<1>		
E5	CUMULUS_VSTM<2>		
F7	CUMULUS_VSTM<3>		
E6	CUMULUS_VSTM<4>		
E7	CUMULUS_VSTM<5>		
F8	CUMULUS_VSTM<6>		
G9	CUMULUS_VSTM<7>		
D6	CUMULUS_VSTM<8>		
D7	CUMULUS_VSTM<9>		
D8	CUMULUS_VSTM<10>		
F9	CUMULUS_VSTM<11>		
D5	CUMULUS_VSTM<12>		
F6	CUMULUS_VSTM<13>		
F5	CUMULUS_VSTM<14>		
G4	CUMULUS_VSTM<15>		
E8	CUMULUS_VSTM<16>		
G8	CUMULUS_VSTM<17>		
G7	CUMULUS_VSTM<18>		
G6	CUMULUS_VSTM<19>		
G5			
G1	GPIO_1/CK	CUMULUS_M2S_CLK	
D4	GPIO_2/SD	CUMULUS_M2S_SDA	
F2	GPIO_3	DISPLAY_SYNC	
F3	GPIO_4	CUMULUS_M_GPIO_4	
C2	TM_ACS*	NC_CUMULUS_M_TM_ACS_L (NO_TEST=TRUE)	
G3	TM_OVR	I2C_GRAPE_SCL_1V8	

=PP1V8_GRAPE_EXT_SW
R4101 4.7K 1% 1/32W MF 01005
GPIO_SOC2GRAPE_RESET_L

R4106 100K 5% 1/32W MF 01005
R4110 4.7K 1% 1/32W MF 01005

GND: C7 C9 G2

SLAVE CUMULUS

=PP5V25_GRAPE
C4150 1UF 20% 10V X5R 0201

=PP1V8_GRAPE_EXT_SW
C4156 0.1UF 20% 4V X5R 01005

PPVDDCORE_CUMULUS_S (VOLTAGE=1.8V)
C4155 56PF 5% 6.3V NP0-C0G 01005
C4152 2.2UF 20% 4V X5R-CERM 0201

PPVDDANA_CUMULUS_S (VOLTAGE=1.8V)
C4153 2.2UF 20% 4V X5R-CERM 0201
C4154 56PF 5% 6.3V NP0-C0G 01005

=PP1V8_GRAPE_EXT_SW
C4159 0.1UF 20% 4V X5R 01005
C4158 100PF 5% 6.3V CERM 01005

U4150 CUMULUS-C1 WLBGA OMIT_TABLE

Pin	Net	Pin	Net
B9	MT_PANEL_IN<15>	IN0_0	
B8	MT_PANEL_IN<16>	IN1_0	
A9	MT_PANEL_IN<17>	IN2_0	
B7	MT_PANEL_IN<18>	IN3_0	
B6	MT_PANEL_IN<19>	IN4_0	
A8	MT_PANEL_IN<20>	IN5_0	
B5	MT_PANEL_IN<21>	IN6_0	
B4	MT_PANEL_IN<22>	IN7_0	
A7	MT_PANEL_IN<23>	IN8_0	
B3	MT_PANEL_IN<24>	IN9_0	
A6	MT_PANEL_IN<25>	IN10_0	
A3	MT_PANEL_IN<26>	IN11_0	
A5	MT_PANEL_IN<27>	IN12_0	
A4	MT_PANEL_IN<28>	IN13_0	
B2	MT_PANEL_IN<29>	IN14_0	
A2	NC_CUMULUS_S_IN14_1 (NO_TEST=TRUE)	IN14_1	
E4	TP_CUMULUS_S_CS_L	H_CS*	
F1	CLK_GRAPE2STINGER_STEP	H_INT*	
D3	GPIO_GRAPE2STINGER_SYNC	H_SCLK	
D2	GPIO_GRAPE2STINGER_RDY	H_SDI	
E1	GPIO_GRAPE2STINGER_EN	H_SDO	
C4	NC_CUMULUS_S_TCK (NO_TEST=TRUE)	JTAG_TCK	
C3	NC_CUMULUS_S_TDI (NO_TEST=TRUE)	JTAG_TDI	
E2	NC_CUMULUS_S_TDO (NO_TEST=TRUE)	JTAG_TDO	
C6	JTAG_CUMULUS_S_TMS	JTAG_TMS	
E3	CUMULUS_S_BCFG_RTCK	BCFG_RTCK	
D1	CLK_SOC2GRAPE_32K	CLKIN/RESET*	
D9	GPIO_SOC2GRAPE_RESET_L	RSTOVR*	
VSTM_0	CUMULUS_VSTM<20>		
E5	CUMULUS_VSTM<21>		
F7	CUMULUS_VSTM<22>		
E6	CUMULUS_VSTM<23>		
E7	CUMULUS_VSTM<24>		
F8	CUMULUS_VSTM<25>		
G9	CUMULUS_VSTM<26>		
D6	CUMULUS_VSTM<27>		
D7	CUMULUS_VSTM<28>		
D8	CUMULUS_VSTM<29>		
F9	CUMULUS_VSTM<30>		
D5	CUMULUS_VSTM<31>		
F6	CUMULUS_VSTM<32>		
F5	CUMULUS_VSTM<33>		
G4	CUMULUS_VSTM<34>		
E8	CUMULUS_VSTM<35>		
G8	CUMULUS_VSTM<36>		
G7	CUMULUS_VSTM<37>		
G6	CUMULUS_VSTM<38>		
G5	CUMULUS_VSTM<39>		
G1	GPIO_1/CK	CUMULUS_M2S_CLK	
D4	GPIO_2/SD	CUMULUS_M2S_SDA	
F2	GPIO_3	TP_CUMULUS_S_GPIO_3	
F3	GPIO_4	GPIO_GRAPE2STINGER_SHDWN_L	
C2	TM_ACS*	NC_CUMULUS_S_TM_ACS_L (NO_TEST=TRUE)	
G3	TM_OVR		

R4159 4.7K 1% 1/32W MF 01005

GND: C7 C9 G2

HALL EFFECT

FL4124 240-OHM-25%-0.20A-1.0DCR (01005)
GPIO_HALL2PMU_IRQ1 — GPIO_HALL2PMU_IRQ1_FILT

FL4125 70-OHM-300MA (01005-1)
=PP3V0_S2R_HALL — PP3V0_S2R_GRAPE_HALL_FILT (VOLTAGE=3.0V)
C4125 27PF 5% 16V NP0-C0G 01005

=PP1V8_S2R_GRAPE_EXTERNAL_SW
C4196 1.0UF 20% 6.3V X5R 0201-1

=PPVCC_MAIN_GRAPE
C4190 0.1UF 10% 16V X5R-CERM 0201

U4190 SLG5AP1443V TDFN (CRITICAL)
VDD, CAP, ON, GND, D, S

GPIO_SOC2GRAPE_EXT_SW_ON — VCC_MAIN_GRAPE_RAMP
C4193 4700PF 10% 16V X7R 201 (CRITICAL)
R4194 100K 5% 1/32W MF 01005
PP1V8_GRAPE_EXT_SW
C4195 10UF 20% 6.3V X5R 0402-10 (CRITICAL)

LAYOUT NOTE: PUT THERMAL VIAS AROUND U4100 IN CASE OF SHORTED CONDITION

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PAGE TITLE: GRAPE: CUMULUS
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REVISION: B.0.0
BRANCH:
PAGE: 41 OF 155
SHEET: 30 OF 73

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DISPLAY CONNECTOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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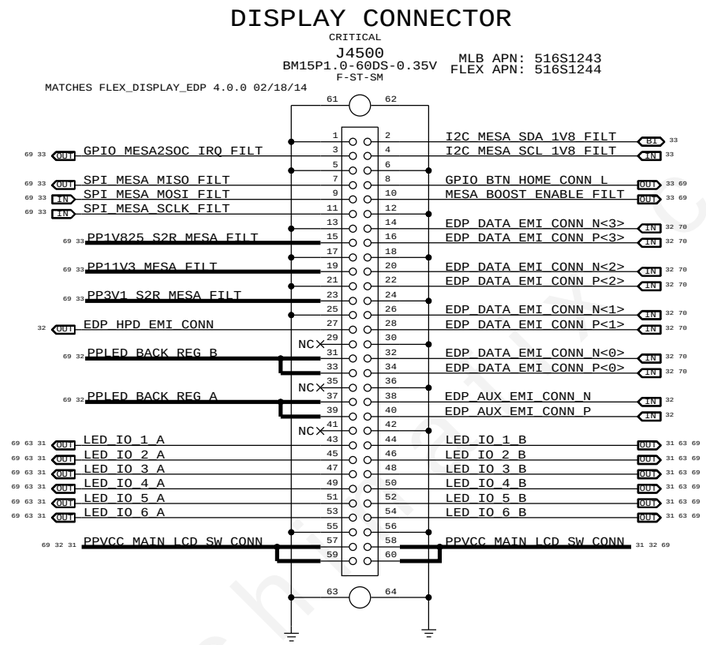
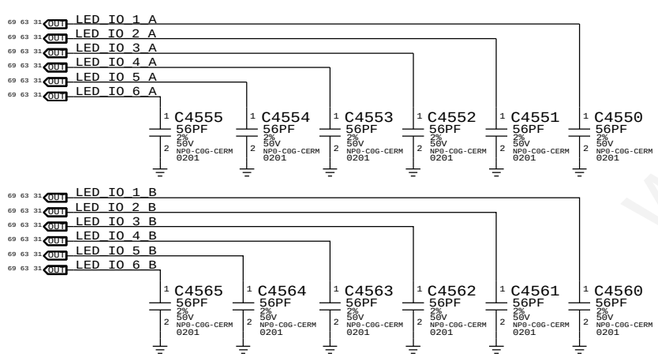


SWAPPED LED STRING A AND B INTENTIONALLY TO EASE ROUTING



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PAGE TITLE
DISPLAY: CONNECTOR

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DRAWING NUMBER 051-0301 SIZE D
REVISION B.0.0
BRANCH
PAGE 45 OF 155
SHEET 31 OF 73

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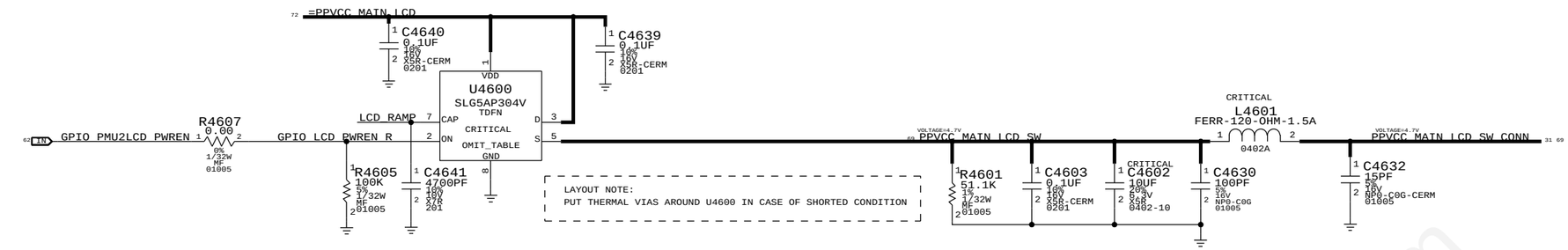
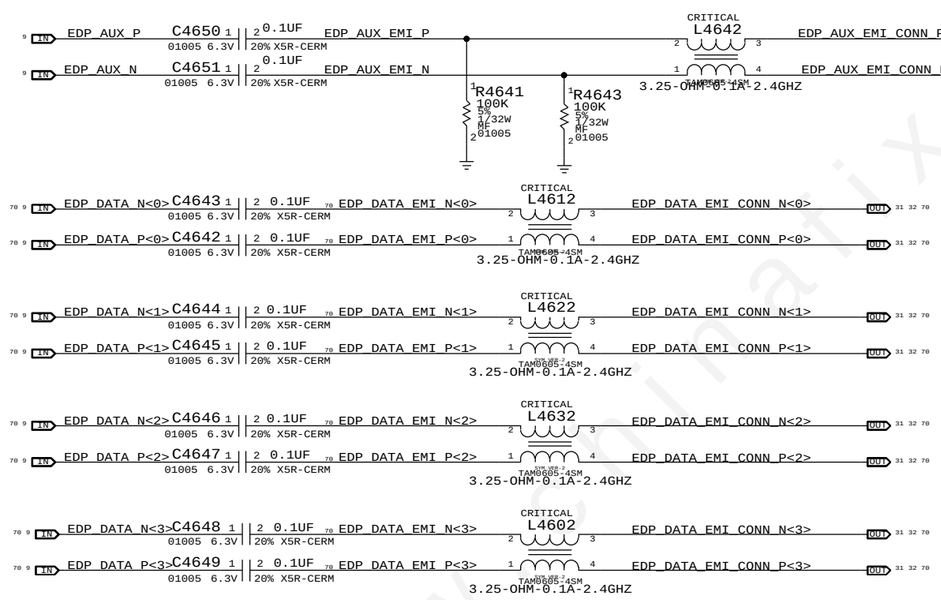
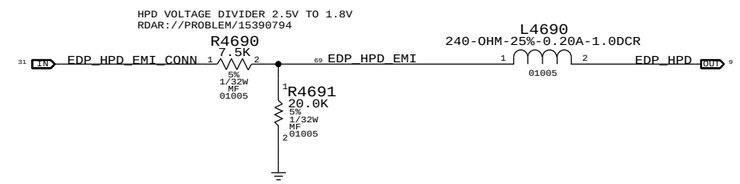
EDP CONNECTOR SUPPORT

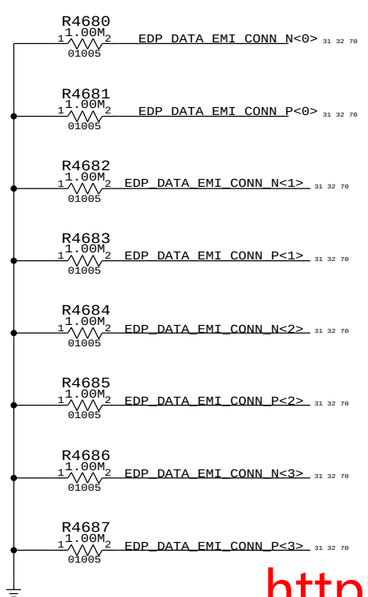
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0914	155S0897	?	L4602, ECT	RDAR://PROBLEM/15954071

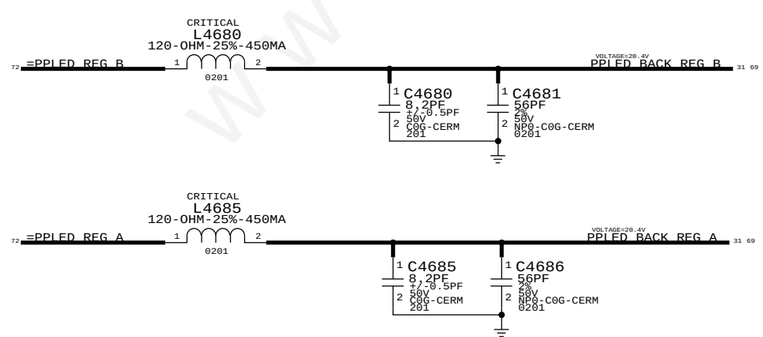


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S4272	1	IC,SLG5AP1423V	U4600	CRITICAL	?









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PAGE TITLE: DISPLAY: EDP SUPPORT

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BRANCH:

PAGE: 46 OF 155

SHEET: 32 OF 73

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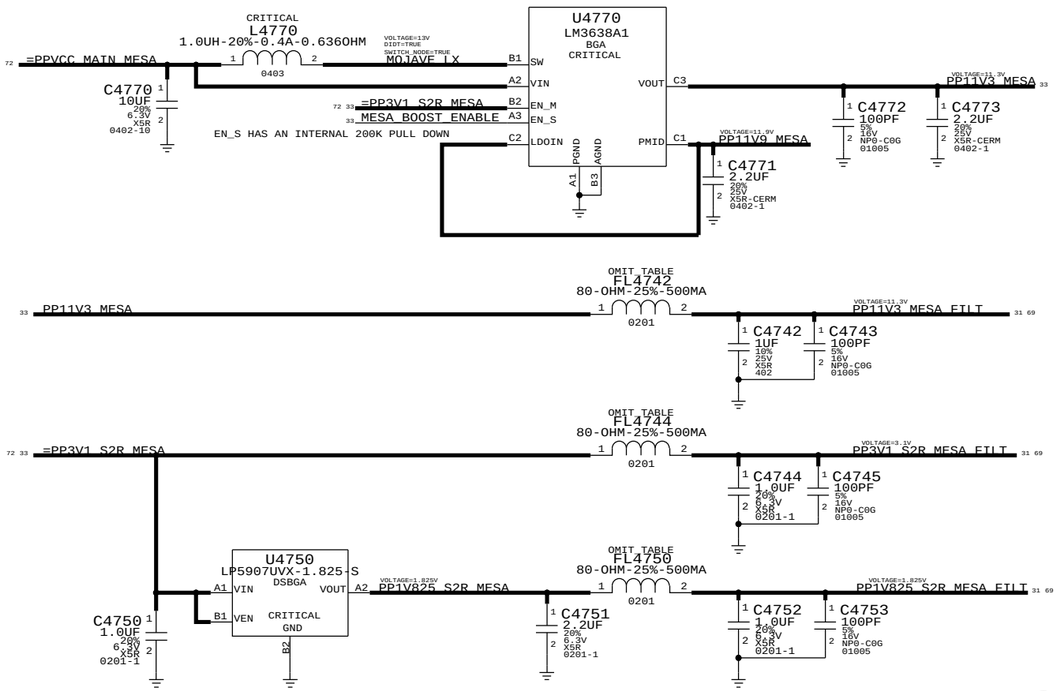
PART#	REV	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
855S00018	3	FERRITE,800OHM,25%,500MA,0.18OHM	FL4742,FL4744,FL4750	CRITICAL	

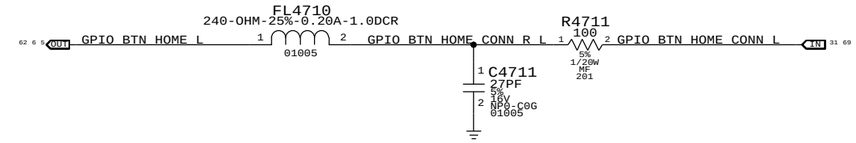
MESA & HOME BUTTON

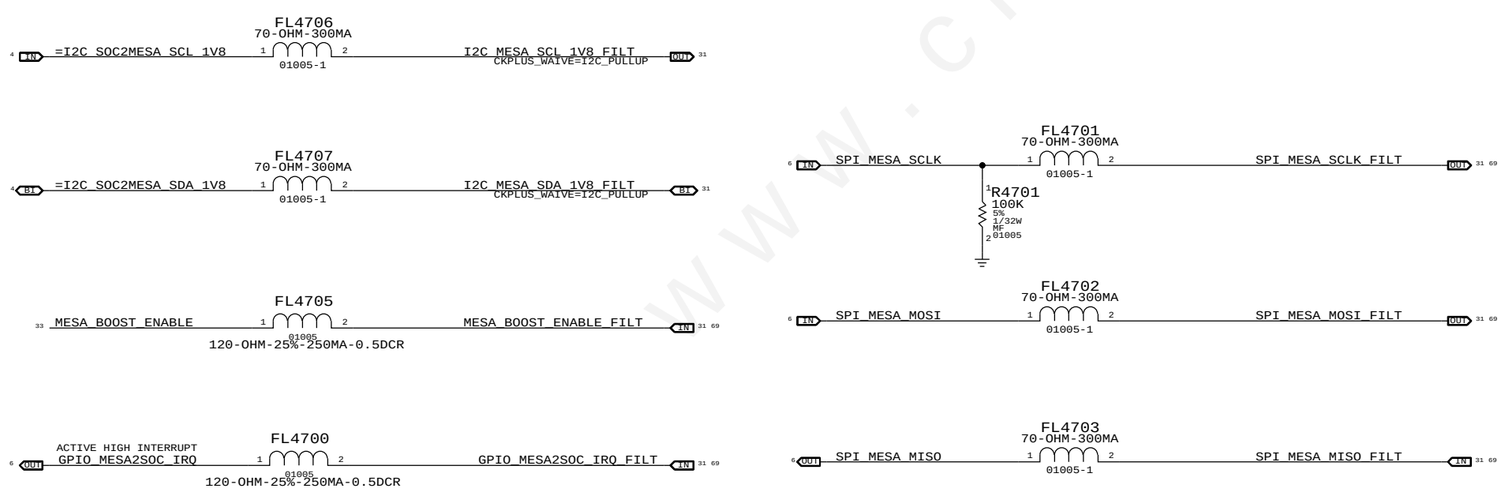
MOJAVE

USING A1 BECAUSE NAVAJO NEEDS 11V3



HOME BUTTON FILTERS





PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00017	155S0755			RDAR://PROBLEM/15807137

FL3910,FL3911,FL4124,L4690,FL4710

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00018	155S0664			RDAR://PROBLEM/15796569

FL2800,FL2802,FL2803,FL2861,FL2871,FL2881,FL2891,FL4742,FL4744,FL4750,FL7900

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: MESA: SUPPORT

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DRAWING NUMBER: 051-0301 SIZE: D

REVISION: B.0.0

BRANCH:

PAGE: 47 OF 155

SHEET: 33 OF 73

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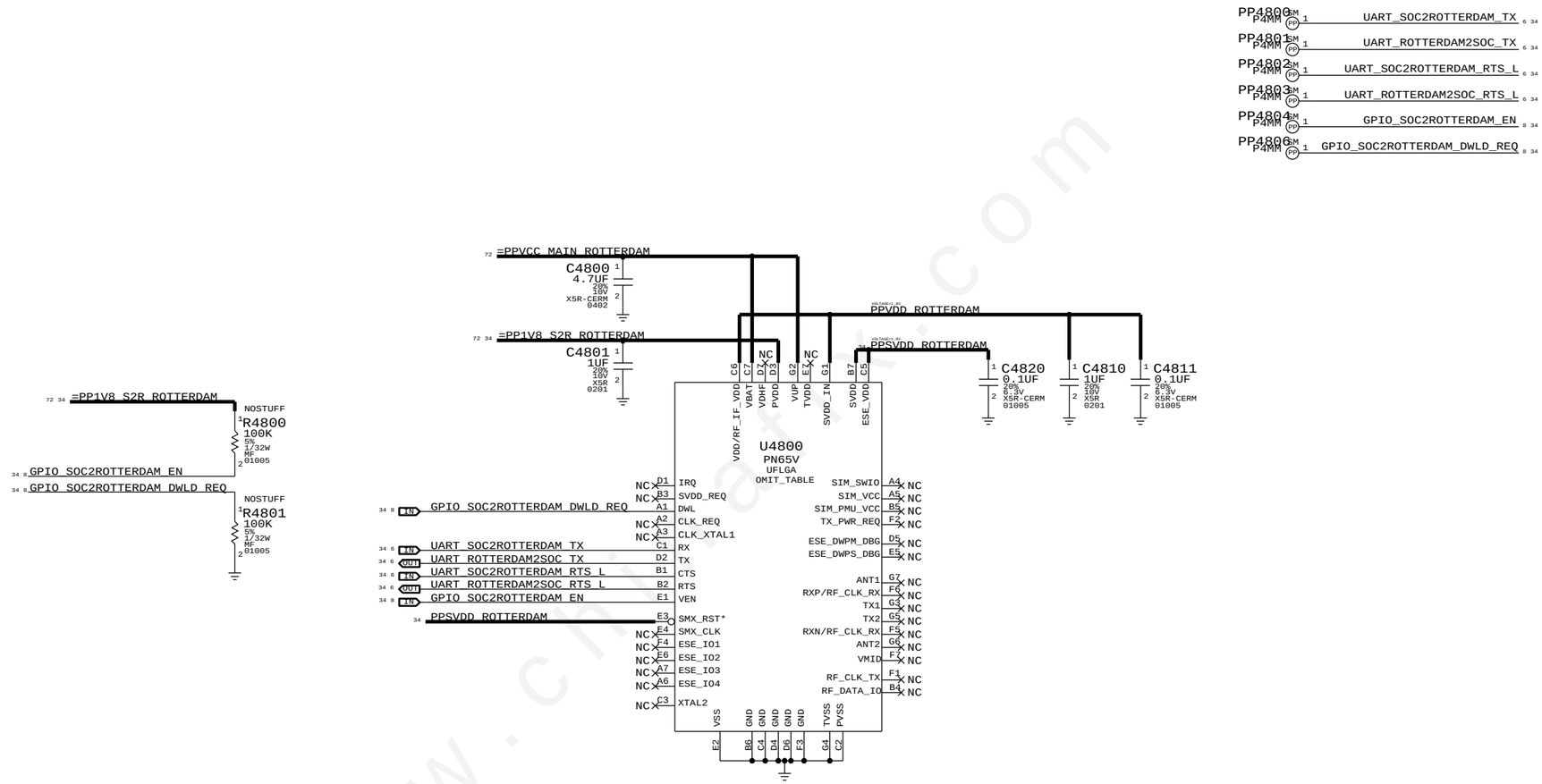
J82 - ROTTERDAM



PAGE TITLE	ROTTERDAM
Apple Inc.	DRAWING NUMBER 051-0301 SIZE D
	REVISION B.0.0
	BRANCH
	PAGE 48 OF 155
	SHEET 34 OF 73

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0043	1	IC,ROTTERDAM,PN,UFLGA	U4800	CRITICAL	

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AP INTERFACE & DEBUG CONNECTOR

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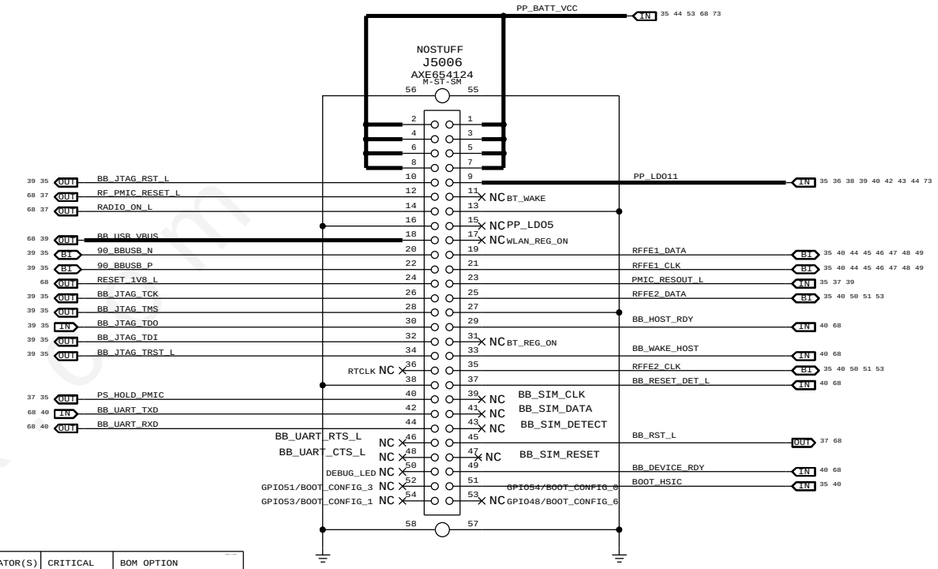
TEST POINTS

TP5000 A 1 50_BB_HSIC_STROBE 39 68
TP5001 A 1 50_BB_HSIC_DATA 39 68
TP5002 A 1 BB_DEBUG_ERROR 40
TP5003 A 1 PS_HOLD_PMIC 35 37
TP5004 A 1 PMIC_RESOUT_L 35 37 39
TP5005 A 1 MDM_CLK 37 39
TP5006 A 1 PP_LDO11 35 36 38 39 40 42 43 44 73
TP5007 A 1 SPMI_DATA 37 39
TP5008 A 1 SPMI_CLK 37 39
TP5025 A 1 BOUNDARY_SCAN_EN 39 69
TP5021 A 1 PP_BATT_VCC 35 44 53 68 73
TP5028 A 1
TP5026 A 1
TP5027 A 1
TP5009 A 1 BB_JTAG_RST_L 35 39
TP5010 A 1 BB_JTAG_TCK 35 39
TP5011 A 1 BB_JTAG_TMS 35 39
TP5012 A 1 BB_JTAG_TDO 35 39
TP5013 A 1 BB_JTAG_TDI 35 39
TP5014 A 1 BB_JTAG_TRST_L 35 39
TP5015 A 1 BB_DEBUG_STATUS 40
TP5016 A 1 BOOT_HSIC 35 40
TP5017 A 1 RFFE1_CLK 35 40 44 45 46 47 48 49
TP5018 A 1 RFFE1_DATA 35 40 44 45 46 47 48 49
TP5019 A 1 RFFE2_CLK 35 40 50 51 53
TP5020 A 1 RFFE2_DATA 35 40 50 51 53
TP5031 A 1 90_BBUSB_N 35 39
TP5030 A 1 90_BBUSB_P 35 39

PROBE POINTS

PP5000 P4MM SM PP 1 SLEEP_CLK_32K 37 39
PP5001 P4MM SM PP 1 BB_EEPROM_SCL 39 40
PP5002 P4MM SM PP 1 BB_EEPROM_SDA 39 40
PP5003 P4MM SM PP 1 ET_DAC_P 40 44
PP5004 P4MM SM PP 1 ET_DAC_N 40 44
TP5029 A 1 PP_LDO6 36 69 71 73

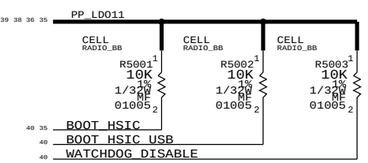
DEBUG CONNECTOR



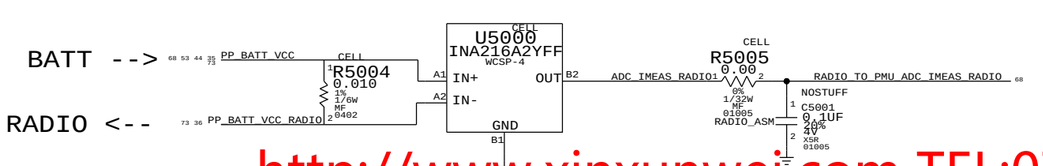
CONFIG _RF BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S0273	1	0.8PF 0201	C6001	CRITICAL	X137_RF
131S0273	1	0.8PF 0201	C6001	CRITICAL	X202_RF
131S0431	1	0.2PF 0201	C6013	CRITICAL	X190_RF
131S0273	1	0.8PF 0201	C6013	CRITICAL	X137_RF
131S0273	1	0.8PF 0201	C6013	CRITICAL	X202_RF
152S2020	1	3.6NH +/-0.1NH 400MA 0201	L6001	CRITICAL	X190_RF
152S2022	1	4.3NH 3% 500MA 0201	L6001	CRITICAL	X137_RF
152S2022	1	4.3NH 3% 500MA 0201	L6001	CRITICAL	X202_RF
131S0323	1	1.1PF 0201	C6421	CRITICAL	X190_RF
152S1217	1	1.0NH +/-0.1NH 750MA 0201	L6402	CRITICAL	X190_RF
152S2042	1	1.8NH +/-0.1NH 800MA 0201	L6402	CRITICAL	X137_RF
152S2042	1	1.8NH +/-0.1NH 800MA 0201	L6402	CRITICAL	X202_RF
152S1994	1	6.8NH 3% 210MA 01005	C6202	CRITICAL	X190_RF
152S1977	1	10.0NH 3% 170MA 01005	C6202	CRITICAL	X137_RF
152S1994	1	6.8NH 3% 210MA 01005	C6202	CRITICAL	X202_RF
152S00028	1	22NH 3% 120MA 01005	L6720	CRITICAL	X190_RF
152S1979	1	18NH 1% 140MA 01005	L6720	CRITICAL	X137_RF
152S1979	1	18NH 1% 140MA 01005	L6720	CRITICAL	X202_RF
138S0831	5	MURATA 2.2UF CAPACITOR	C5101,C5121,C5122,C6010,C6011	CRITICAL	CELL

REPLACES 138S0917 - 138S0917 CAN ONLY BE USED ON RAILS WITH 3V OR LESS



PP_VCC_MAIN CURRENT SENSE



BOM ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1850	152S1721		L5101,L5103,L5104	MURATA IN, 2.2UH, 2016
152S2050	152S1857		L5902	TAIYO IND, 2.2UH, 2012

REVISION DATE: 9/29/2014

SYNC_MASTER=RADIO SYNC_DATE=09/29/2014
PAGE TITLE
CELL: PROBE PTS & DEBUG CONN

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DRAWING NUMBER 051-0301 SIZE D
REVISION B.0.0
BRANCH
PAGE 50 OF 155
SHEET 35 OF 73

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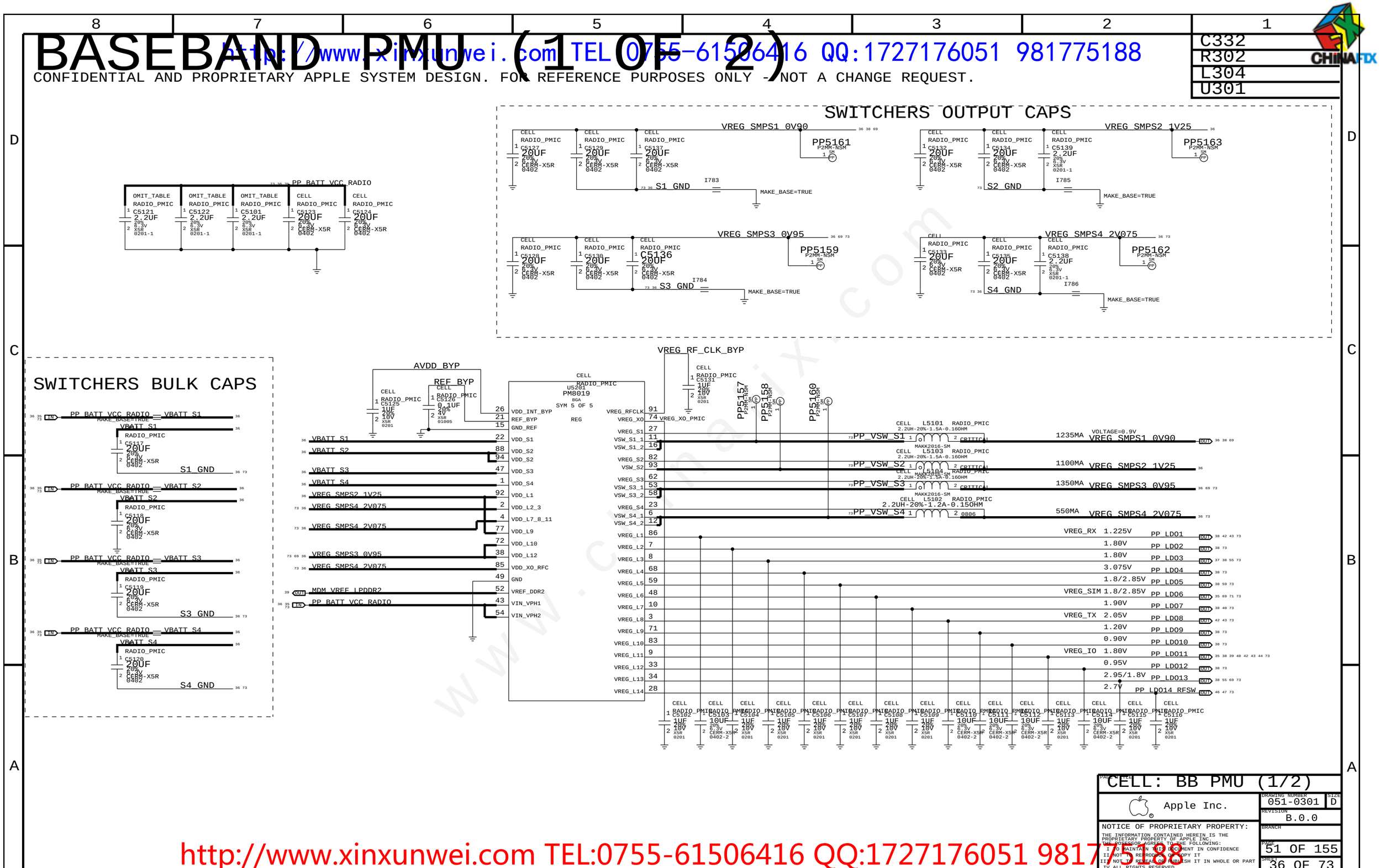
C332
R302
L304
U301



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REVISION B.0.0

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PAGE 51 OF 155

SHEET 36 OF 73

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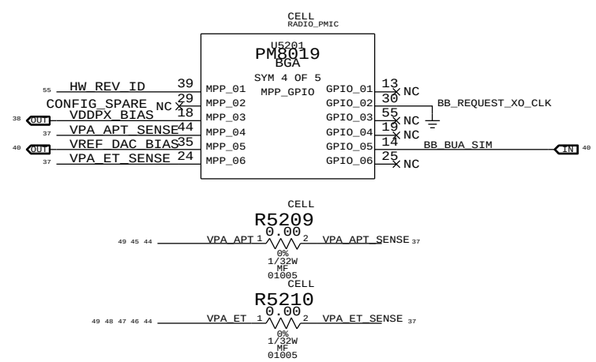
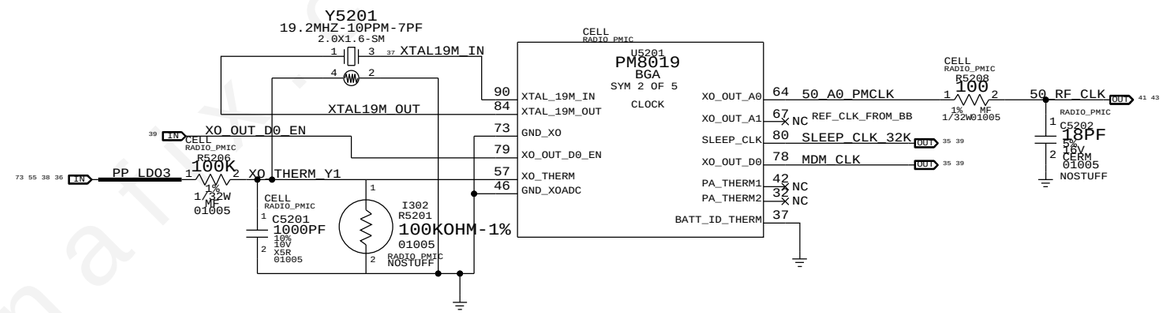
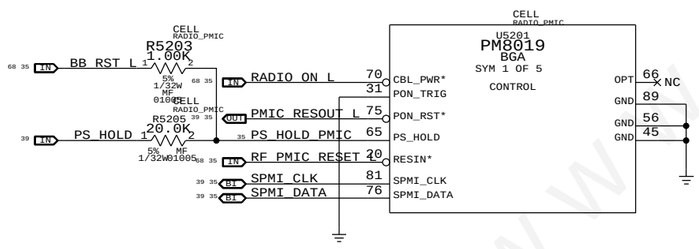
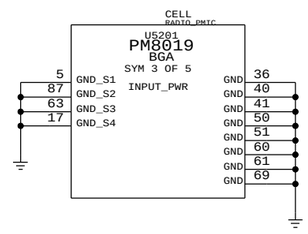
C401
R411
L400
U404

HW_REV_ID	R5202	R5207	J82 REV	J97 REV	J99 REV
0.10V	887K	51.1K	N/A	PROTO0	N/A
0.20V	422K	51.1K	PROTO0	PROTO0B	PROTO0
0.30V	255K	51.1K	PROTO1	PROTO1	PROTO1
0.40V	178K	51.1K	PROTO2		
0.50V	255K	100K	EVT		
0.60V	102K	51.1K	DVT		
0.70V	82.5K	51.1K	PVT		









PAGE TITLE	
CELL: BB PMU (2/2)	
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	REVISION B.0.0
	BRANCH
	PAGE 52 OF 155
	SHEET 37 OF 73

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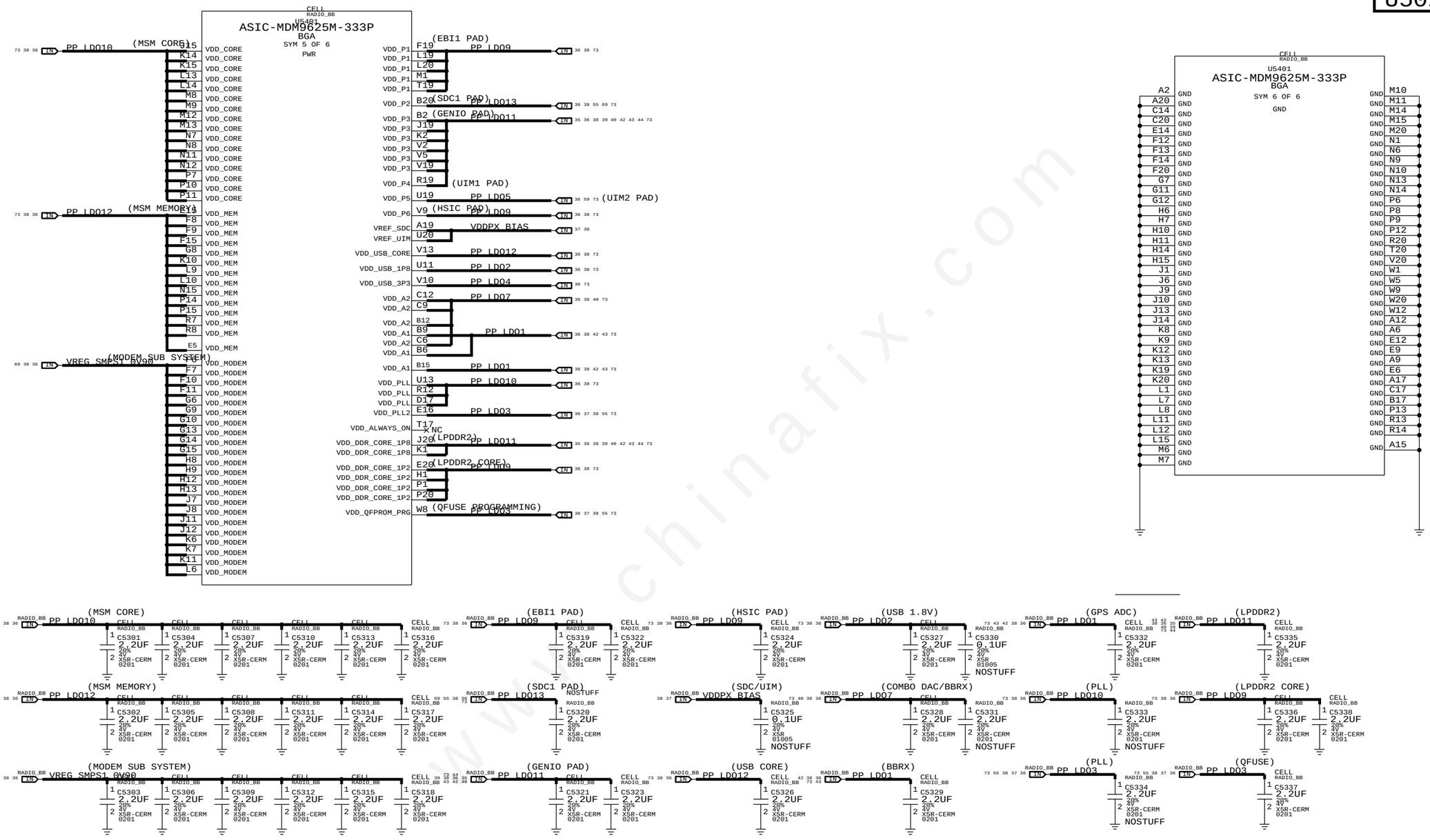
C538
R500
L500
U502



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PAGE 53 OF 155

SHEET 38 OF 73

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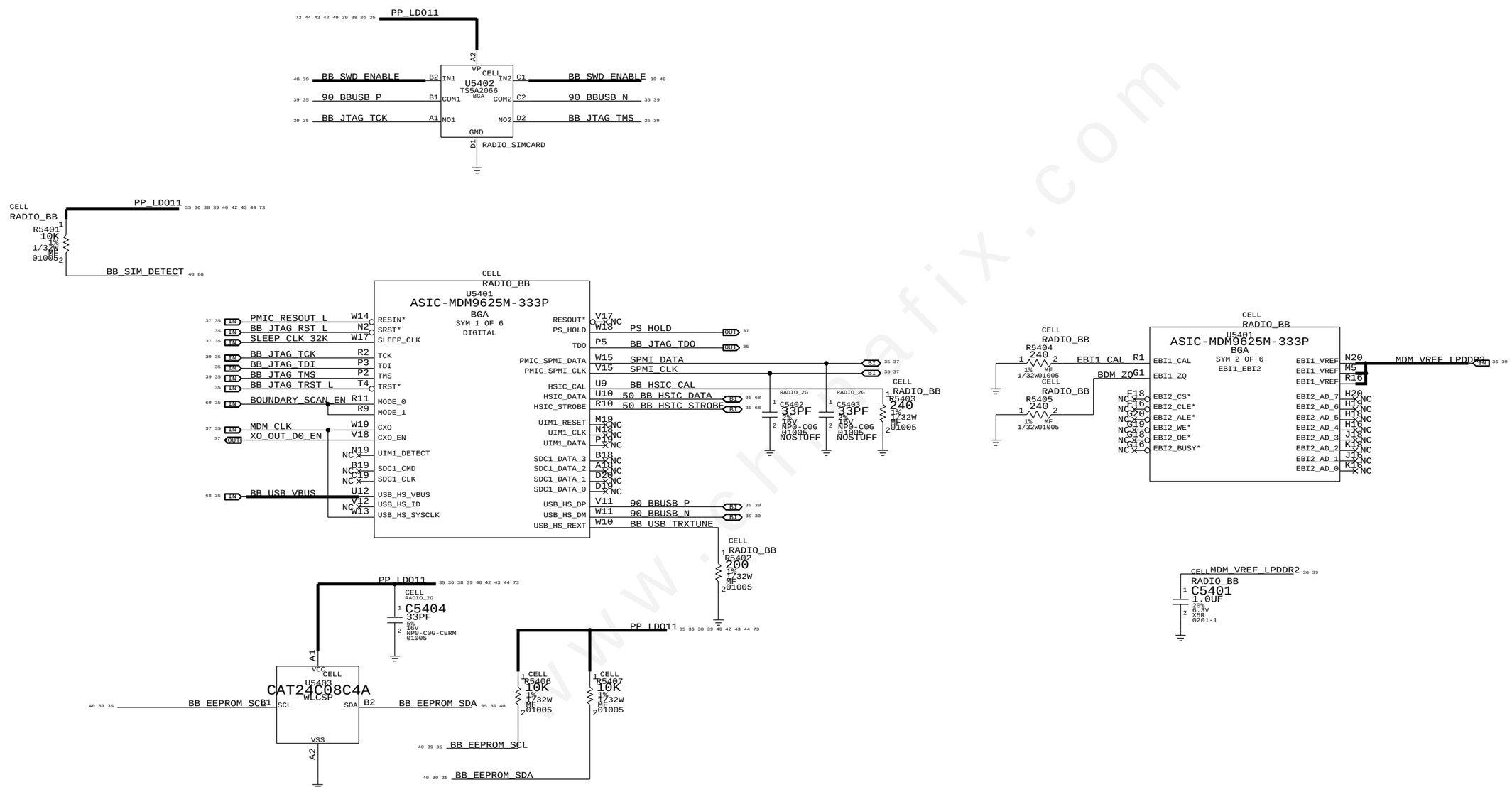
C600
R606
L600
U602



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DRAWING NUMBER 051-0301 SIZE D

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PAGE 54 OF 155

SHEET 39 OF 73

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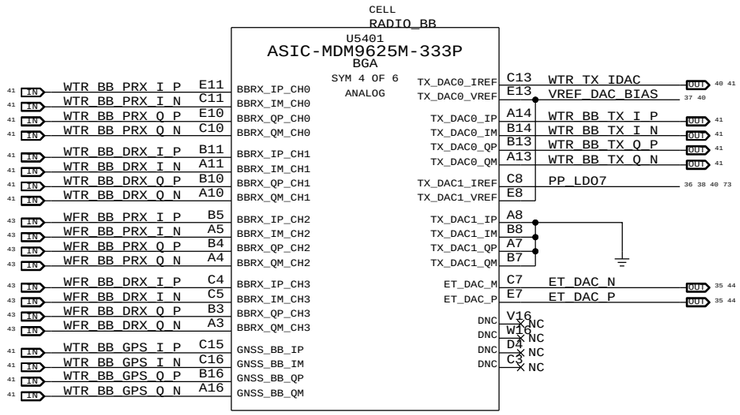
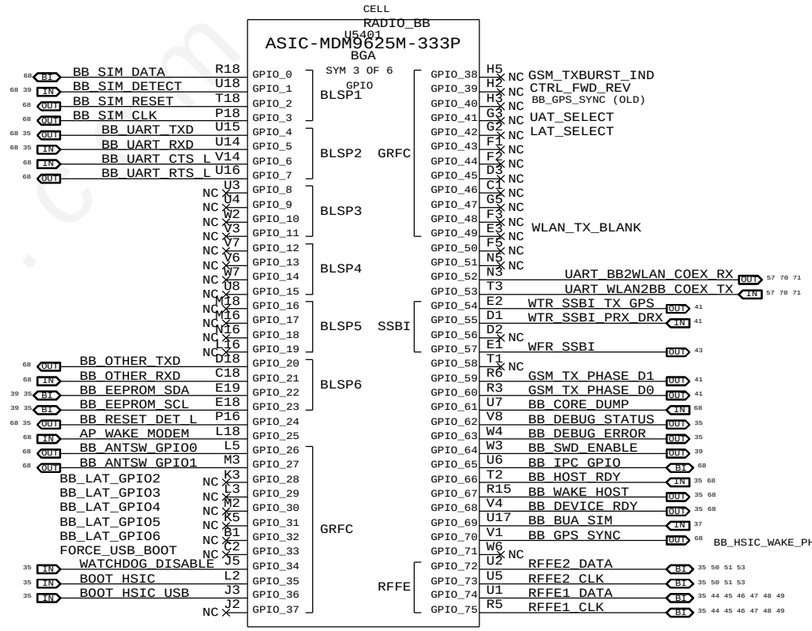
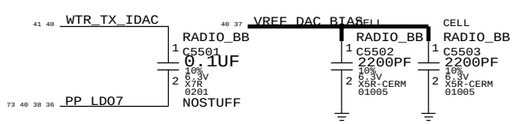
C704
R700
L700
U702







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PAGE 55 OF 155

SHEET 40 OF 73

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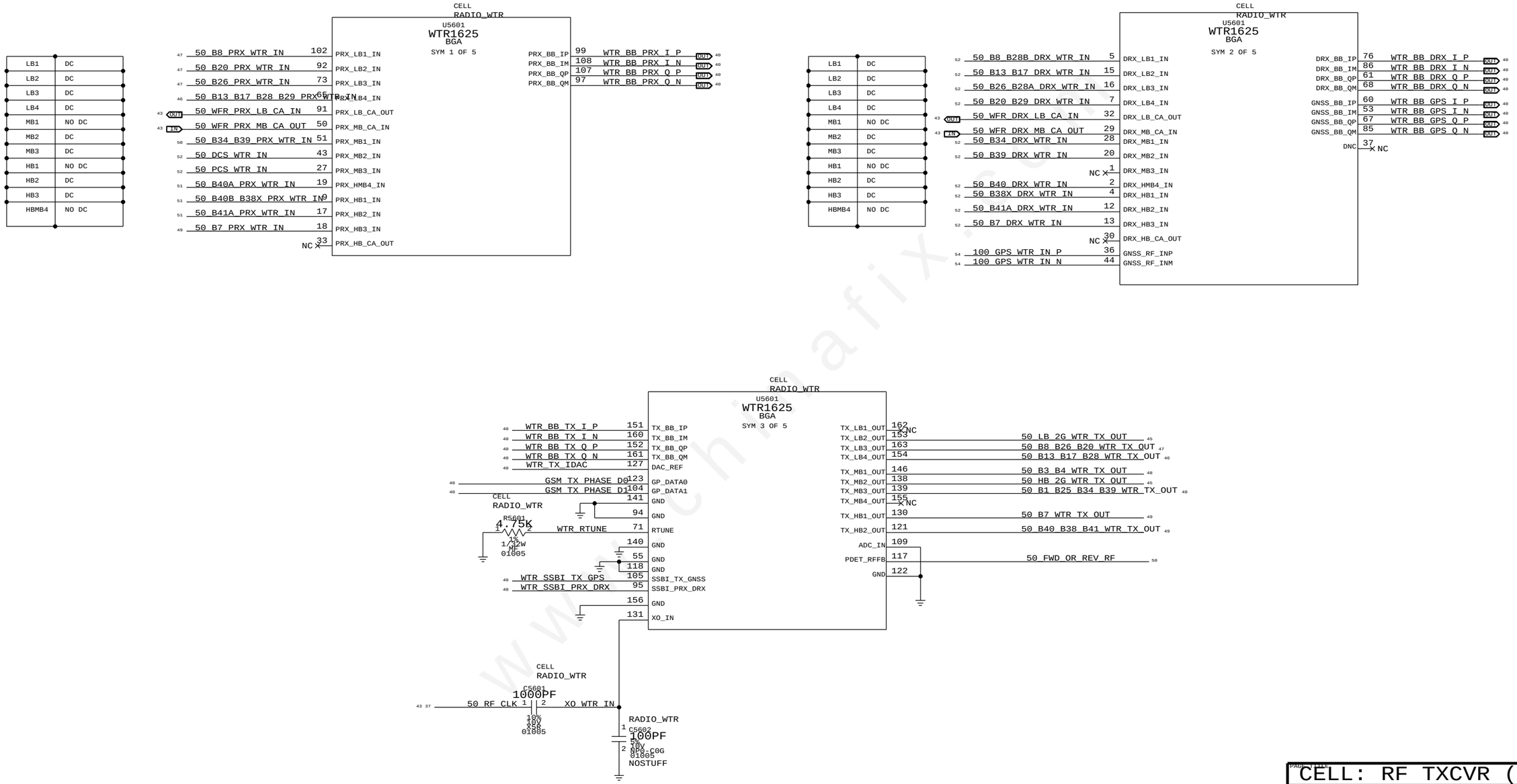
C802
R802
L800
U803



RF_CLK IS SHARED BETWEEN WTR AND WFR. LENGTH DIFFERENCE BETWEEN THE TWO SHOULD BE < 5MM.

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	PAGE 56 OF 155
	SHEET 41 OF 73

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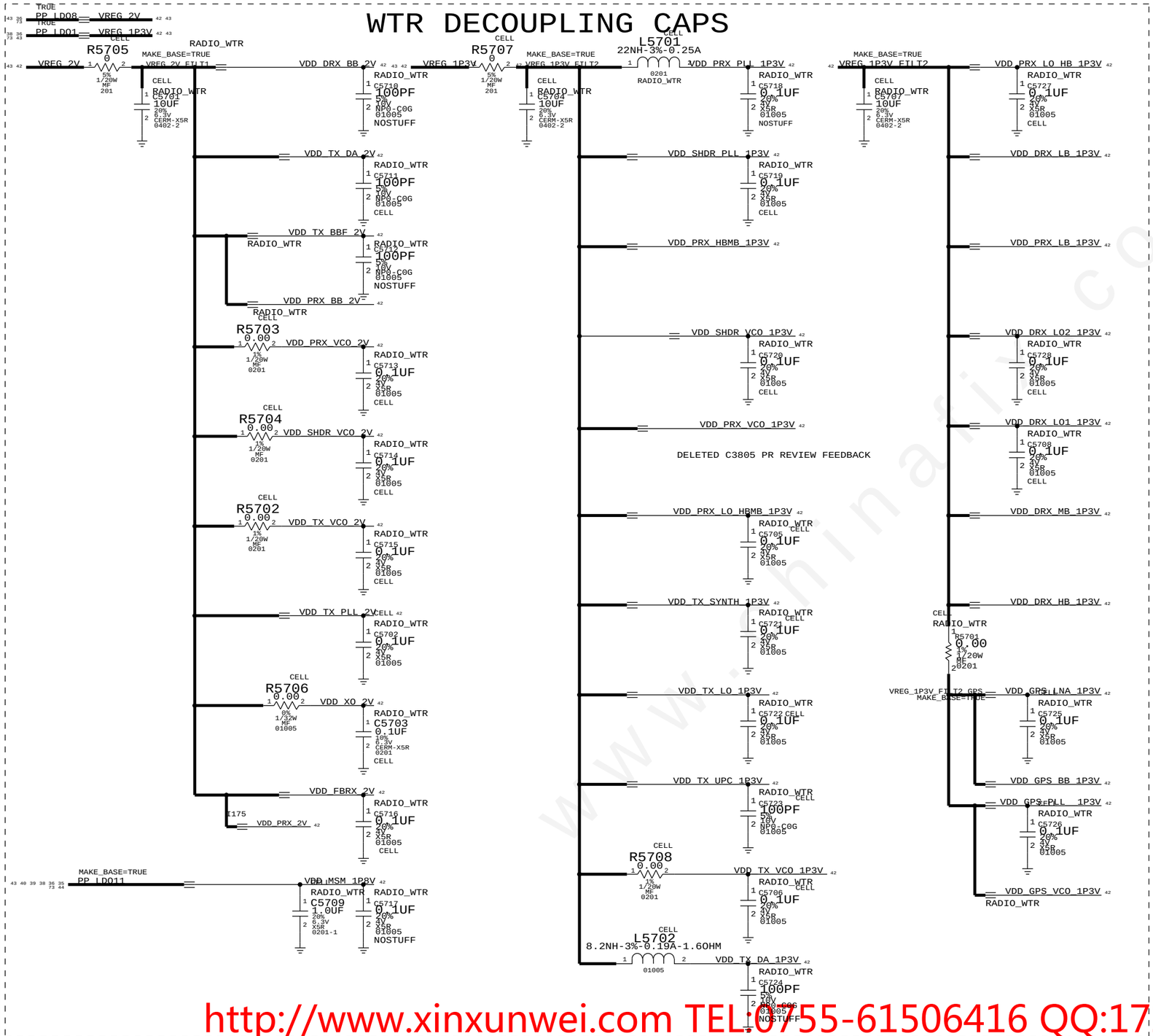
C934
R926
L3802_RF
U902

WTR DECOUPLING CAPS



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PAGE 57 OF 155
SHEET 42 OF 73

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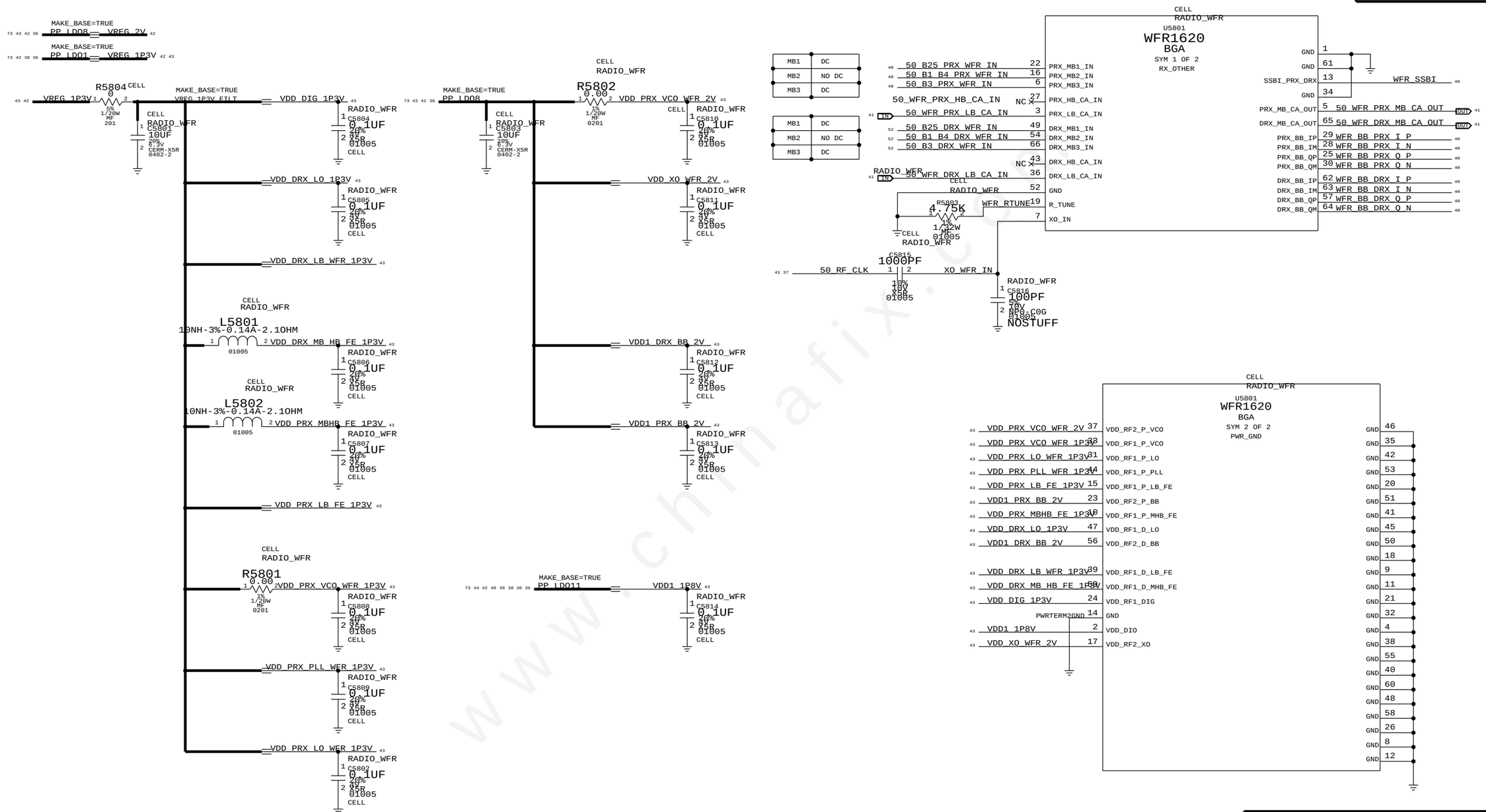
C1019
R1016
L1000
U1002



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	PAGE 58 OF 155
	SHEET 43 OF 73

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QFE DCDC

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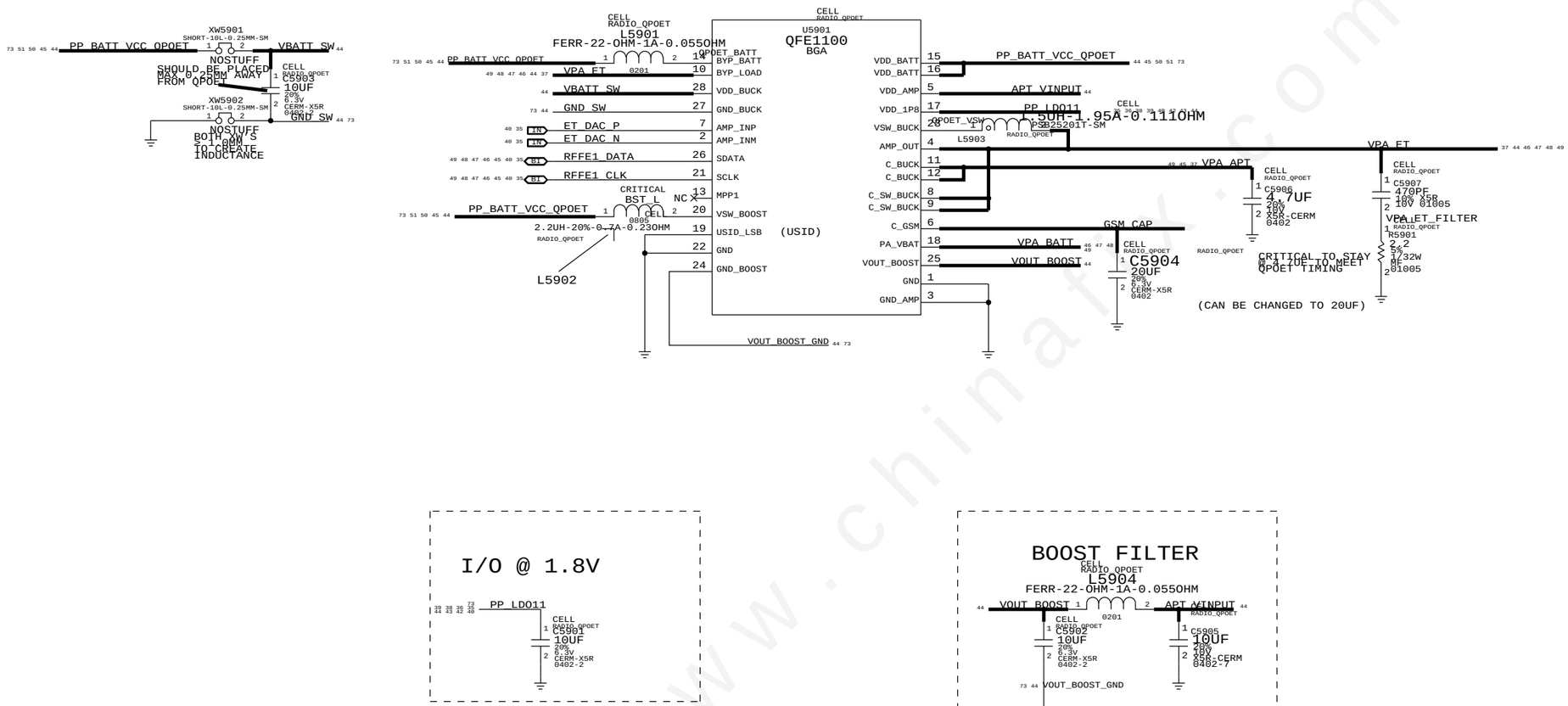
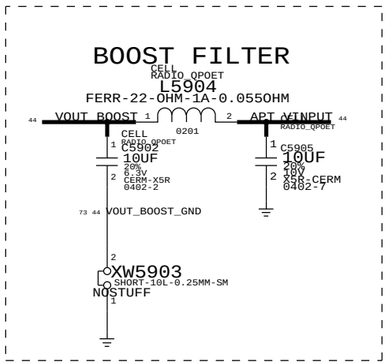
C1110
R1102
L1104
U1101

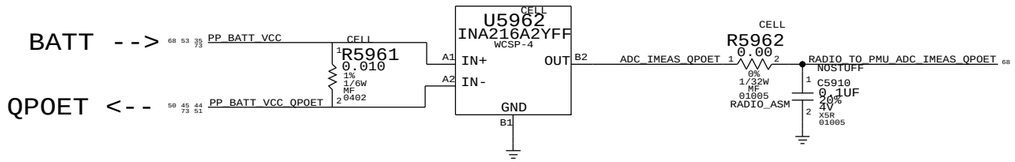


I/O @ 1.8V

BOOST FILTER



PP_VCC_MAIN CURRENT SENSE



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DRAWING NUMBER: 051-0301 SIZE: D

REVISION: B.0.0

BRANCH

PAGE: 59 OF 155

SHEET: 44 OF 73

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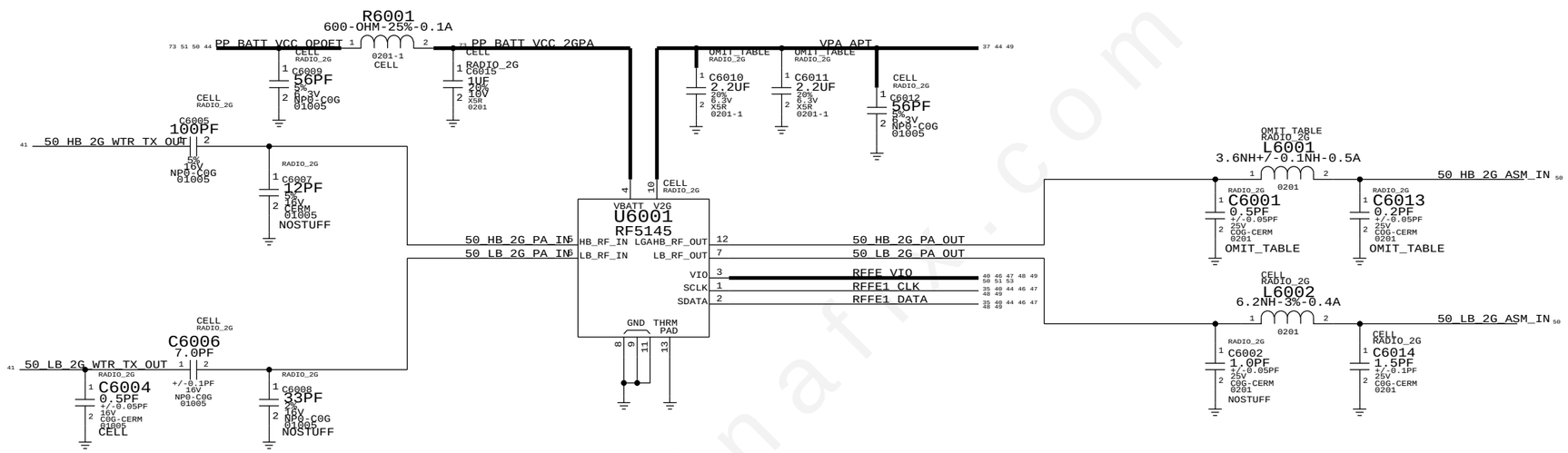
C1208
R1200
L1204
U1201

CHANGE TO VBATT!!!!



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REVISION: B.0.0

BRANCH:

PAGE: 60 OF 155

SHEET: 45 OF 73

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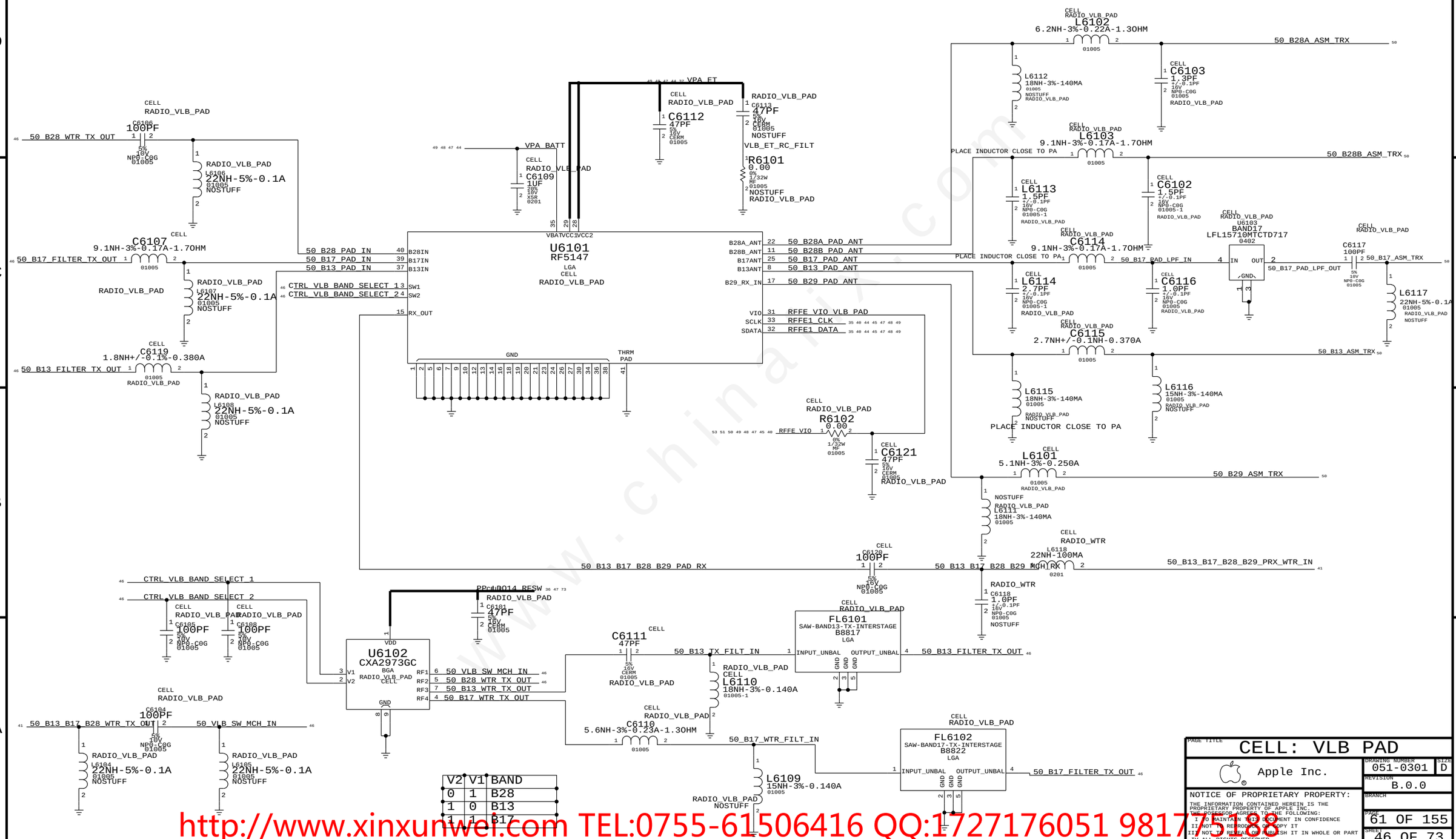
C1332
R1300
L4215_RF
U1304



V2	V1	BAND
0	1	B28
1	0	B13
1	1	B17

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PAGE TITLE: CELL: VLB PAD

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REVISION: B.0.0

BRANCH:

PAGE: 61 OF 155

SHEET: 46 OF 73

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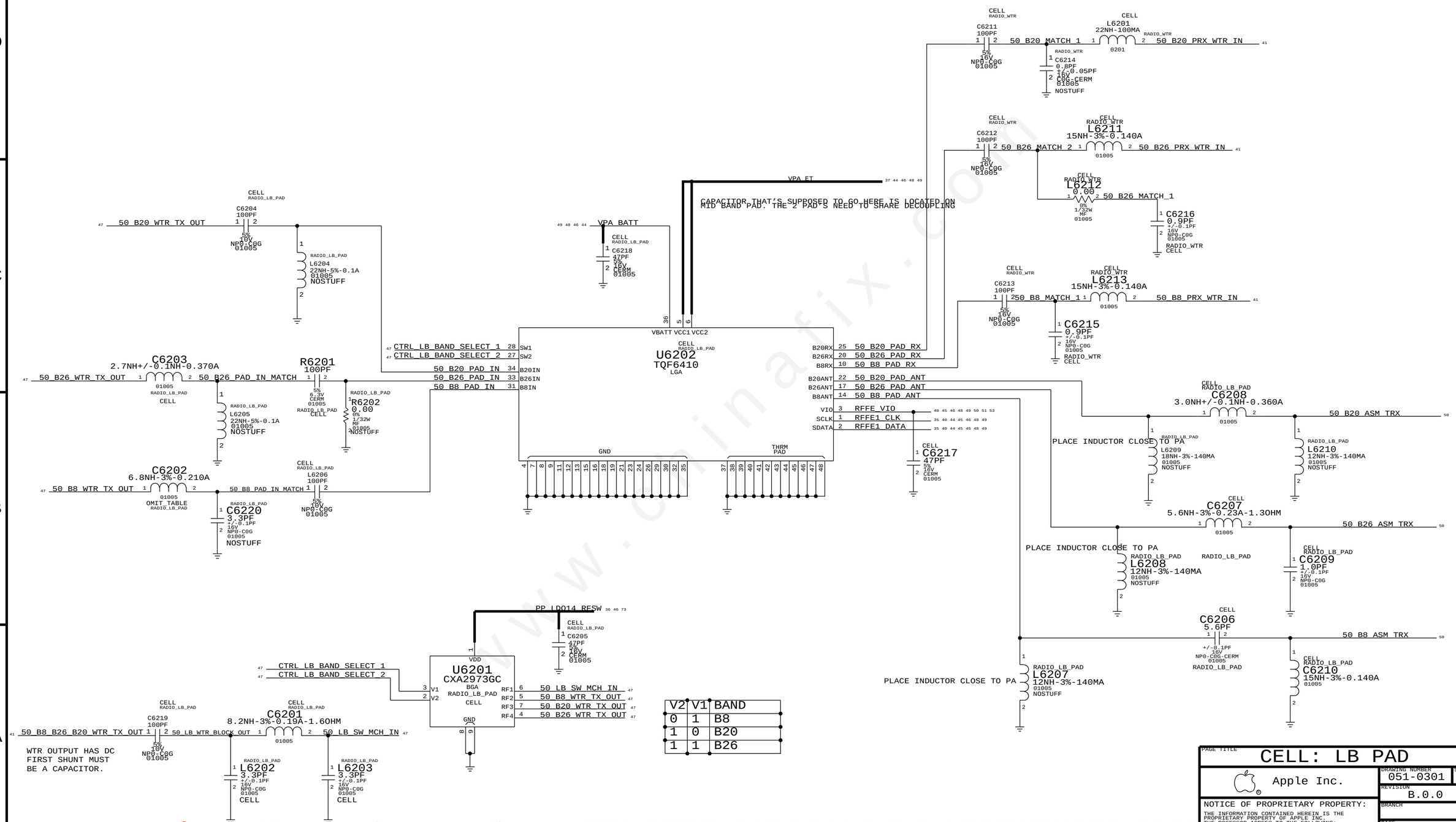
C4317_RF
R1400
L4316_RF
U1402



V2	V1	BAND
0	1	B8
1	0	B20
1	1	B26

PAGE TITLE: CELL: LB PAD

Apple Inc.

DRAWING NUMBER: 051-0301 SIZE: D

REVISION: B.0.0

BRANCH:

PAGE: 62 OF 155

SHEET: 47 OF 73

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MID BAND PAD (B1, B25, B3, B4, B34, B39)

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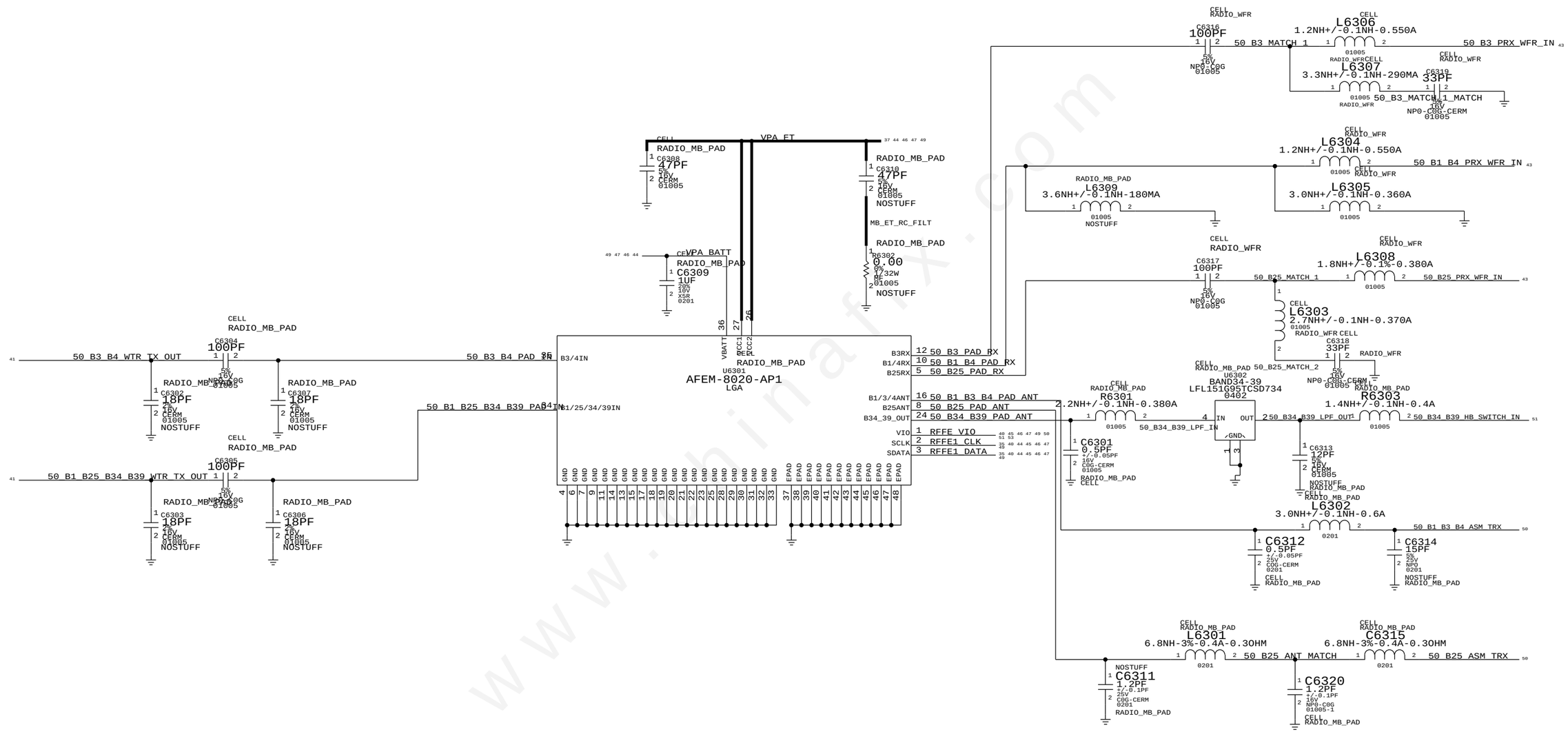
C1510
R1500
L4409_RF
U1501



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PAGE TITLE: CELL: MB PAD

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PAGE: 63 OF 155

SHEET: 48 OF 73

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HIGH BAND PAD (B7, B38, B40, B41, XGP)

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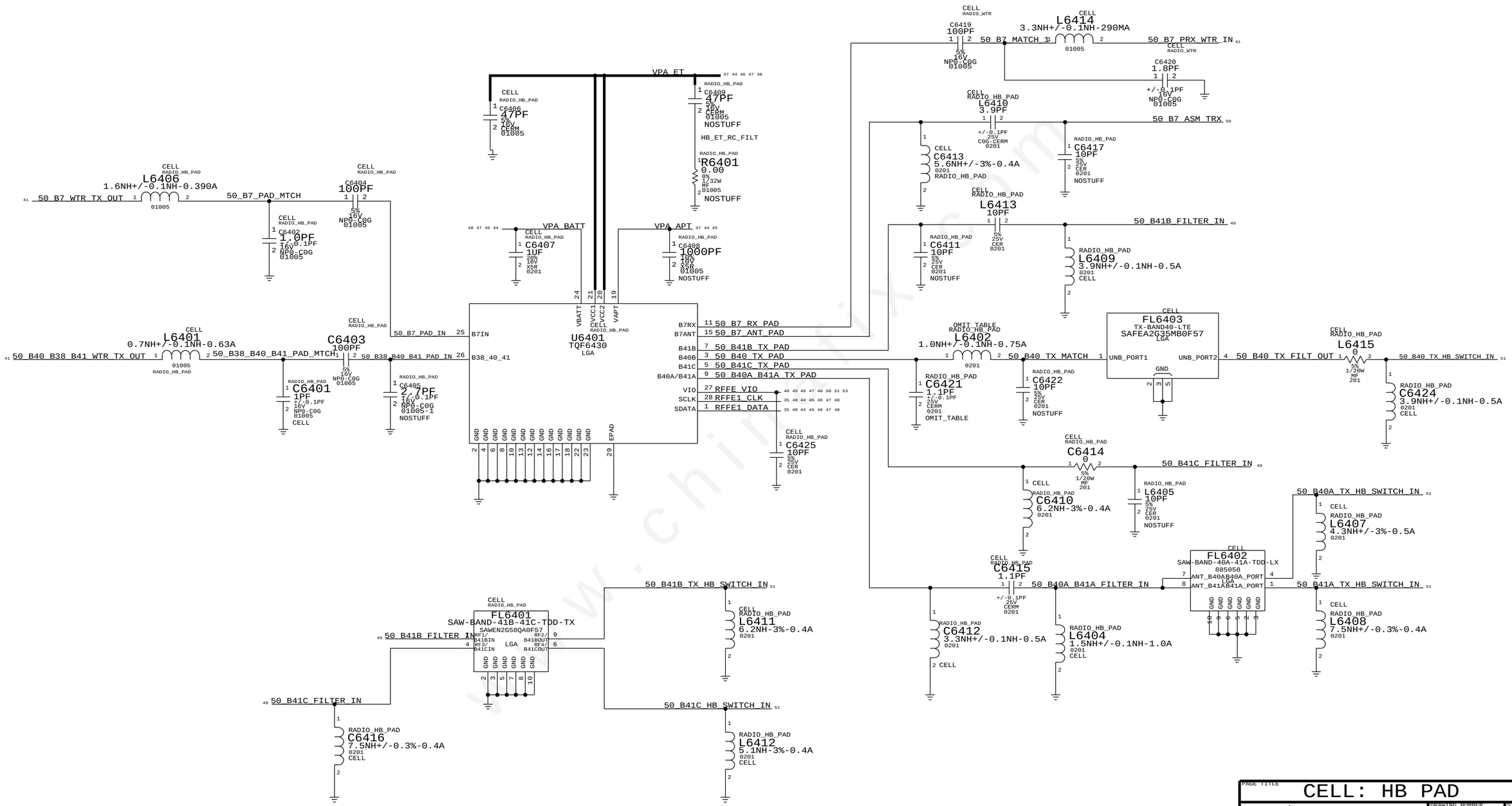
C1614
R1600
L1616
U1601



PAGE TITLE: CELL: HB PAD

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DRAWING NUMBER: 051-0301 SIZE: D

REVISION: B.0.0

BRANCH

PAGE: 64 OF 155

SHEET: 49 OF 73

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ANTENNA SWITCH

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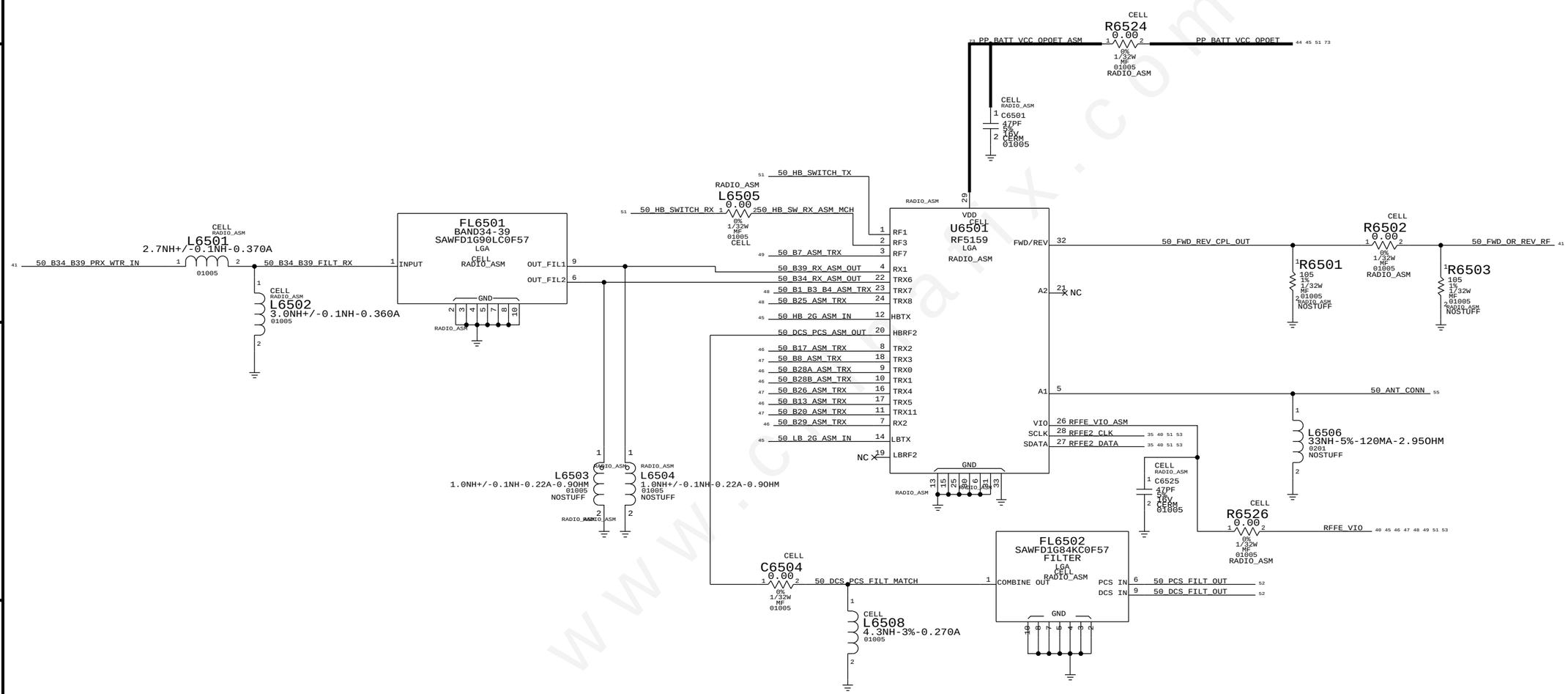
C1702
R1700
L4608_RF
U1702



PAGE TITLE	CELL: ANTENNA SWITCH
	Apple Inc.
DRAWING NUMBER	051-0301
SIZE	D
REVISION	B.0.0
BRANCH	
PAGE	65 OF 155
SHEET	50 OF 73

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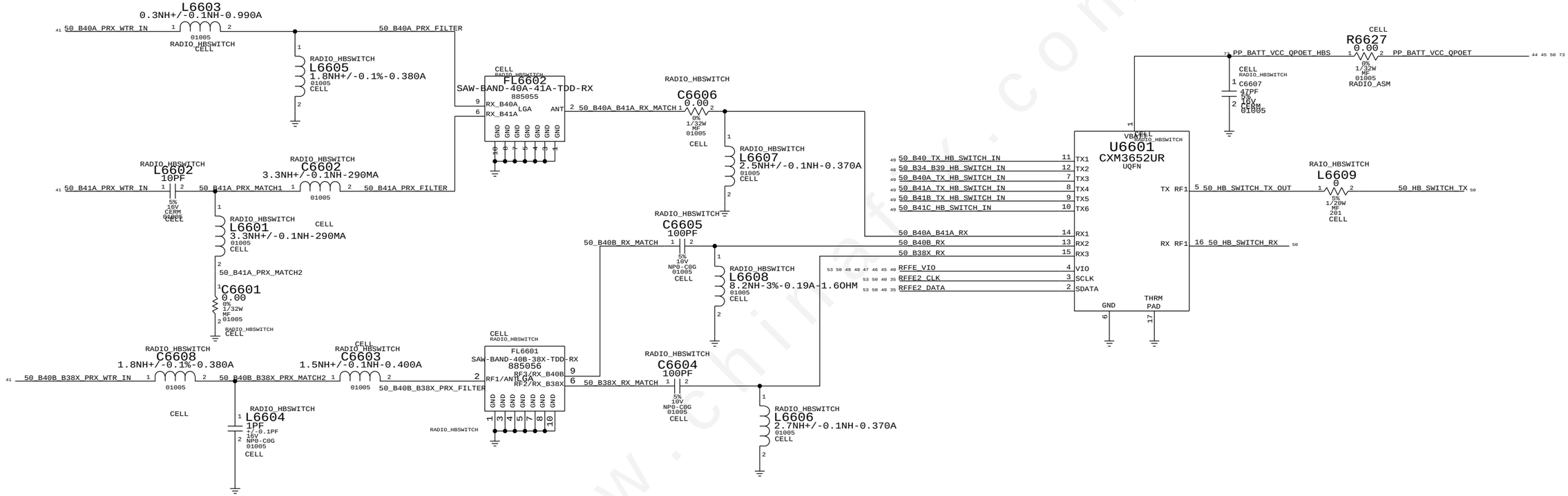

PAGE TITLE	CELL: HB SWITCH
	Apple Inc.
DRAWING NUMBER	051-0301
SIZE	D
REVISION	B.0.0
BRANCH	
PAGE	66 OF 155
SHEET	51 OF 73

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RX DIVERSITY (1 OF 2)

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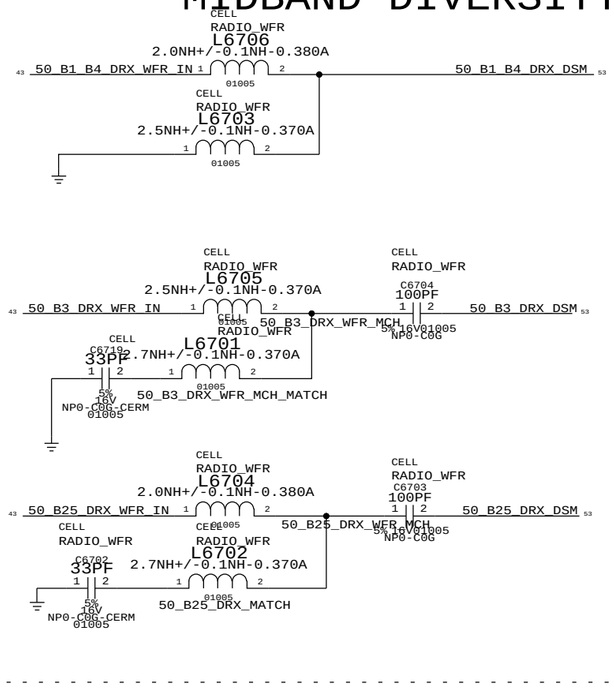
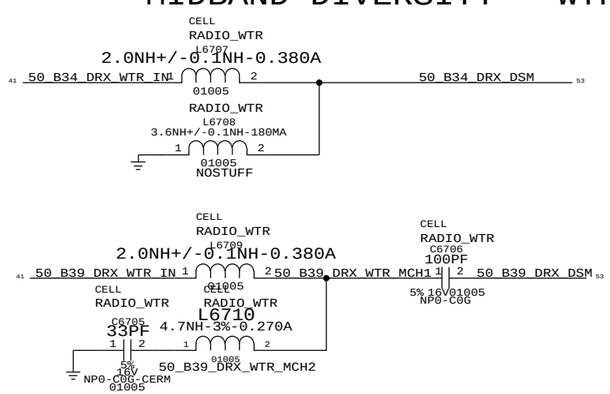
C4826_RF
R1800
L1829
U1801

MIDBAND

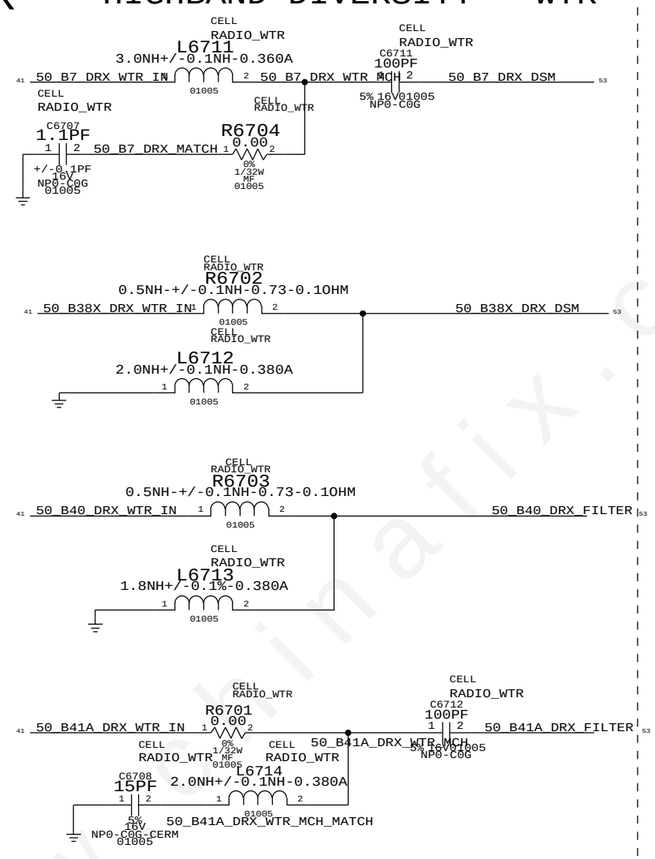
MIDBAND DIVERSITY - WFR

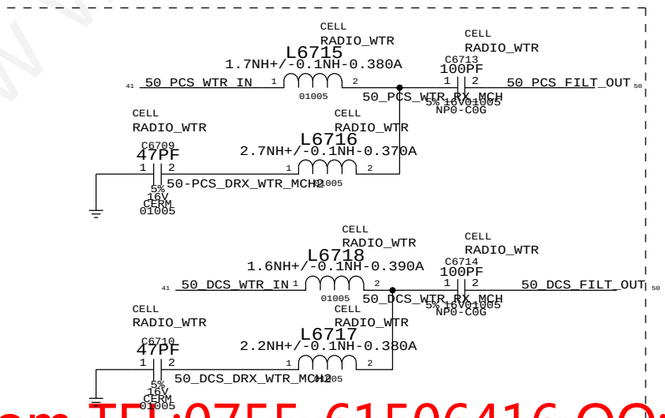


MIDBAND DIVERSITY - WTR

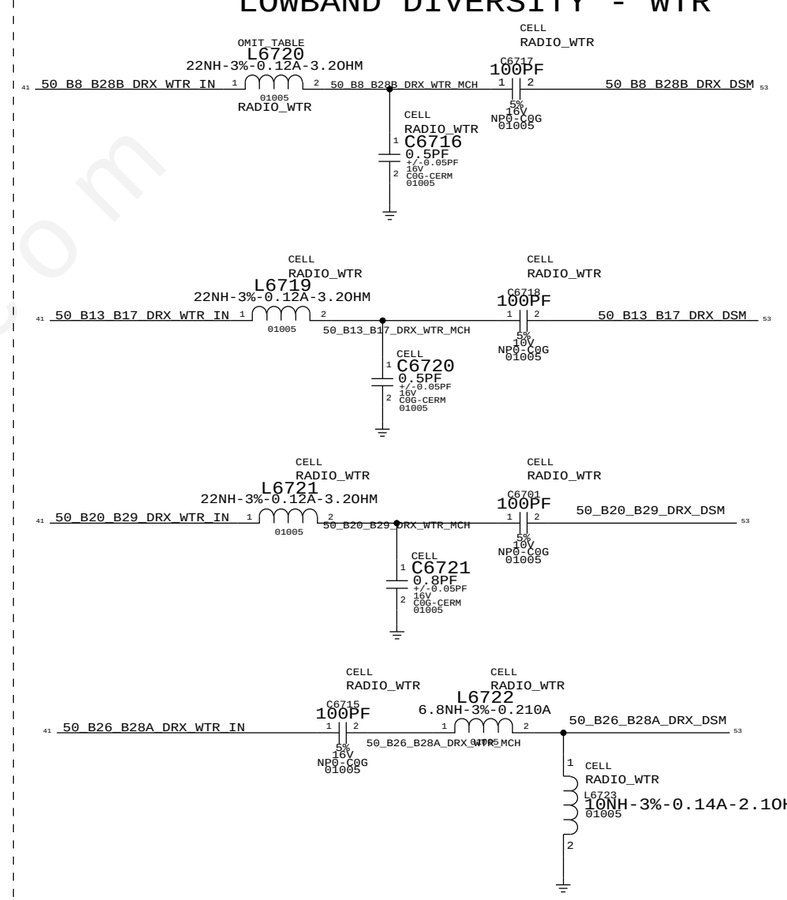


HIGHBAND DIVERSITY - WTR





LOWBAND DIVERSITY - WTR



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PAGE TITLE: CELL: RX DIV (1/2)

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REVISION: B.0.0

BRANCH:

PAGE: 67 OF 155

SHEET: 52 OF 73

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RX DIVERSITY (2 OF 2)

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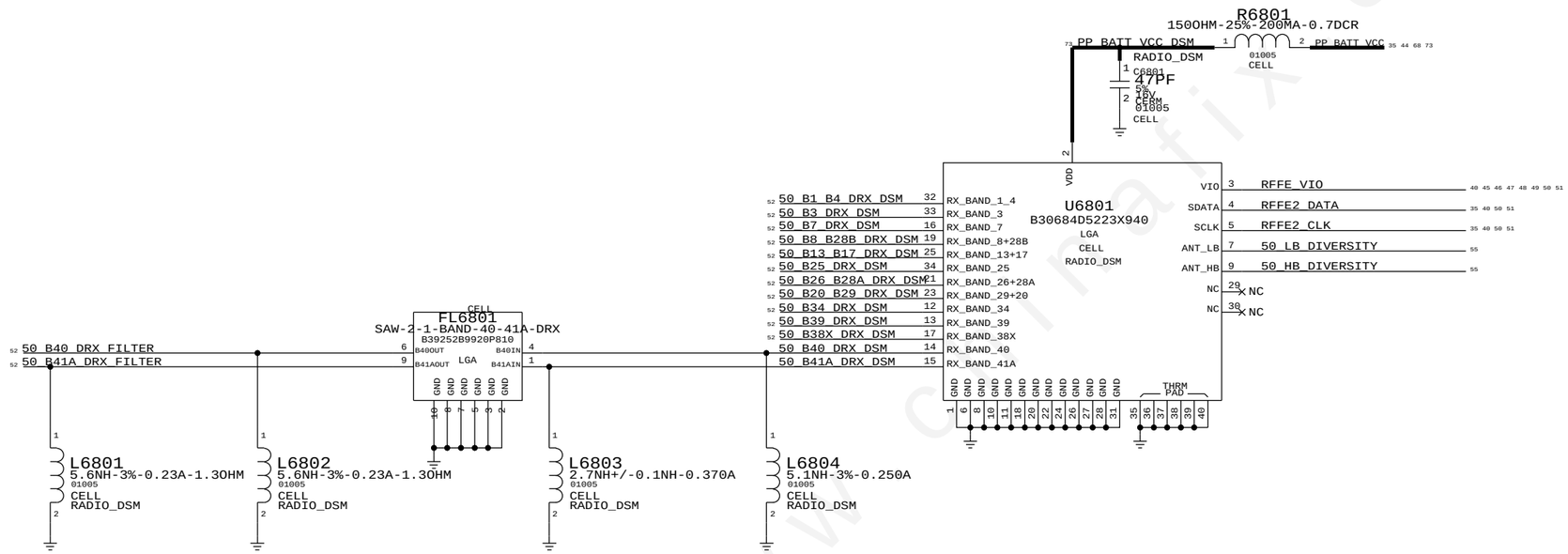
C1900
R1900
L1900
U1901



PAGE TITLE
CELL: RX DIV (2/2)

Apple Inc.

DRAWING NUMBER 051-0301
SIZE D
REVISION B.0.0
BRANCH
PAGE 68 OF 155
SHEET 53 OF 73

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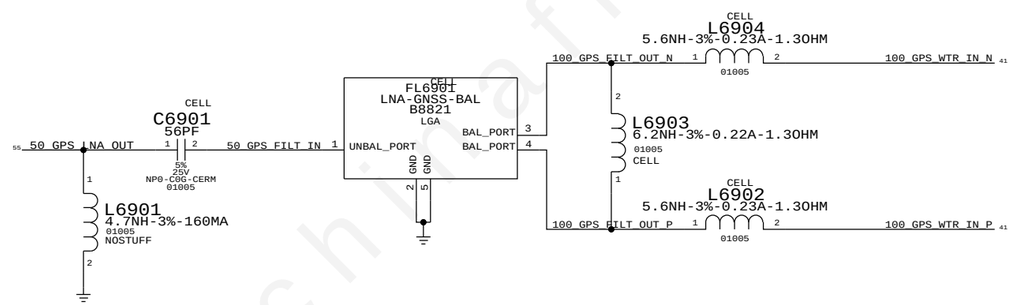

PAGE TITLE	CELL: GPS
Apple Inc.	DRAWING NUMBER 051-0301 SIZE D
	REVISION B.0.0
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	SHEET 54 OF 73

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ANTENNA FEEDS AND GPS (J82)

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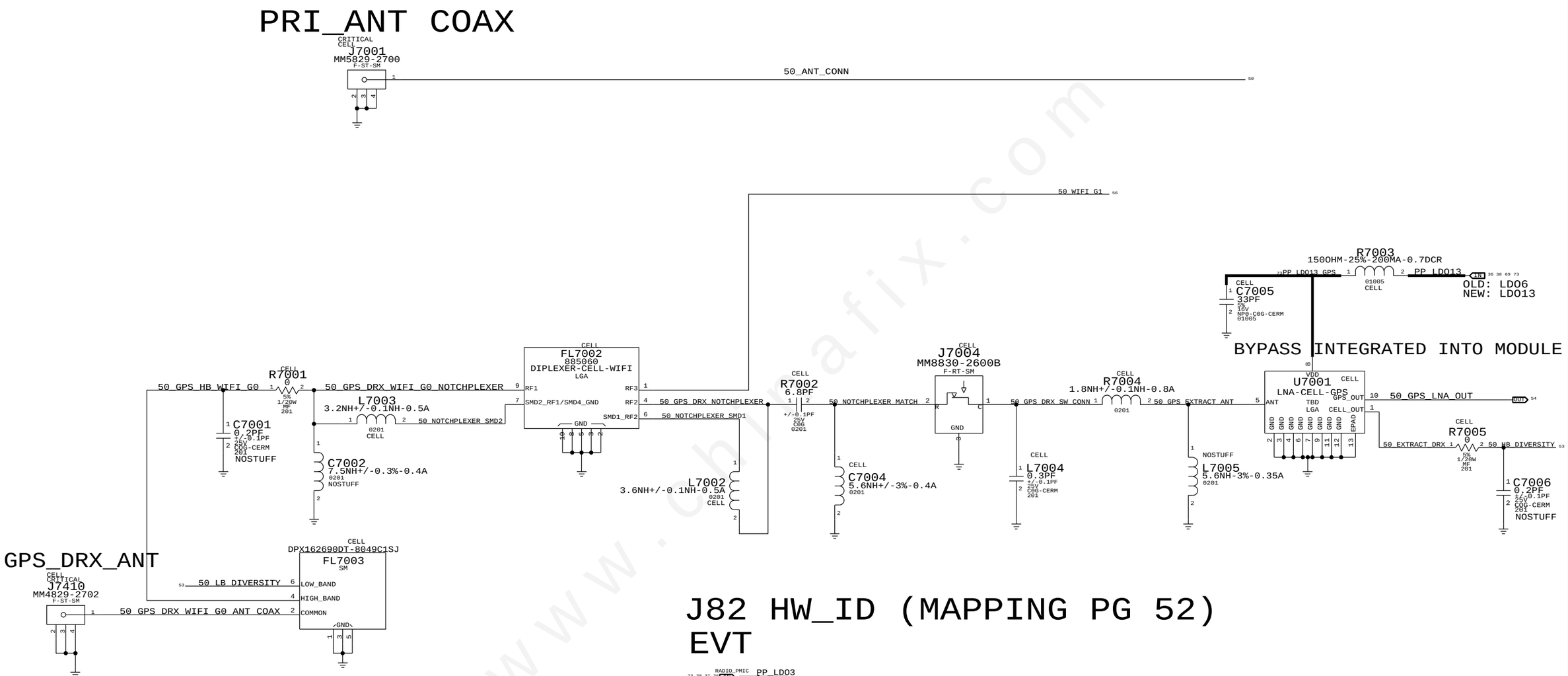

HW_REV_ID	R7010	R7011	J82 REV	J97 REV	J99 REV
0.10V	887K	51.1K	N/A	PROTO0	PROTO0
0.20V	422K	51.1K	PROTO0	PROTO0B	PROTO1
0.30V	255K	51.1K	PROTO1	PROTO1	PROTO2
0.40V	178K	51.1K	PROTO2		
0.50V	255K	100K	PRE-EVT		
0.60V	102K	51.1K	EVT		
0.70V	82.5K	51.1K	DVT		

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0565	197S0598		Y5201	KDS XTAL, 19.2MHZ
197S0593	197S0598		Y5201	NDK XTAL, 19.2MHZ

SYNC DATE=09/29/2014

PAGE TITLE: CELL: ANT FEEDS & GPS (J82)

Apple Inc.

DRAWING NUMBER: 051-0301 SIZE: D

REVISION: B.0.0

BRANCH:

PAGE: 70 OF 155

SHEET: 55 OF 73

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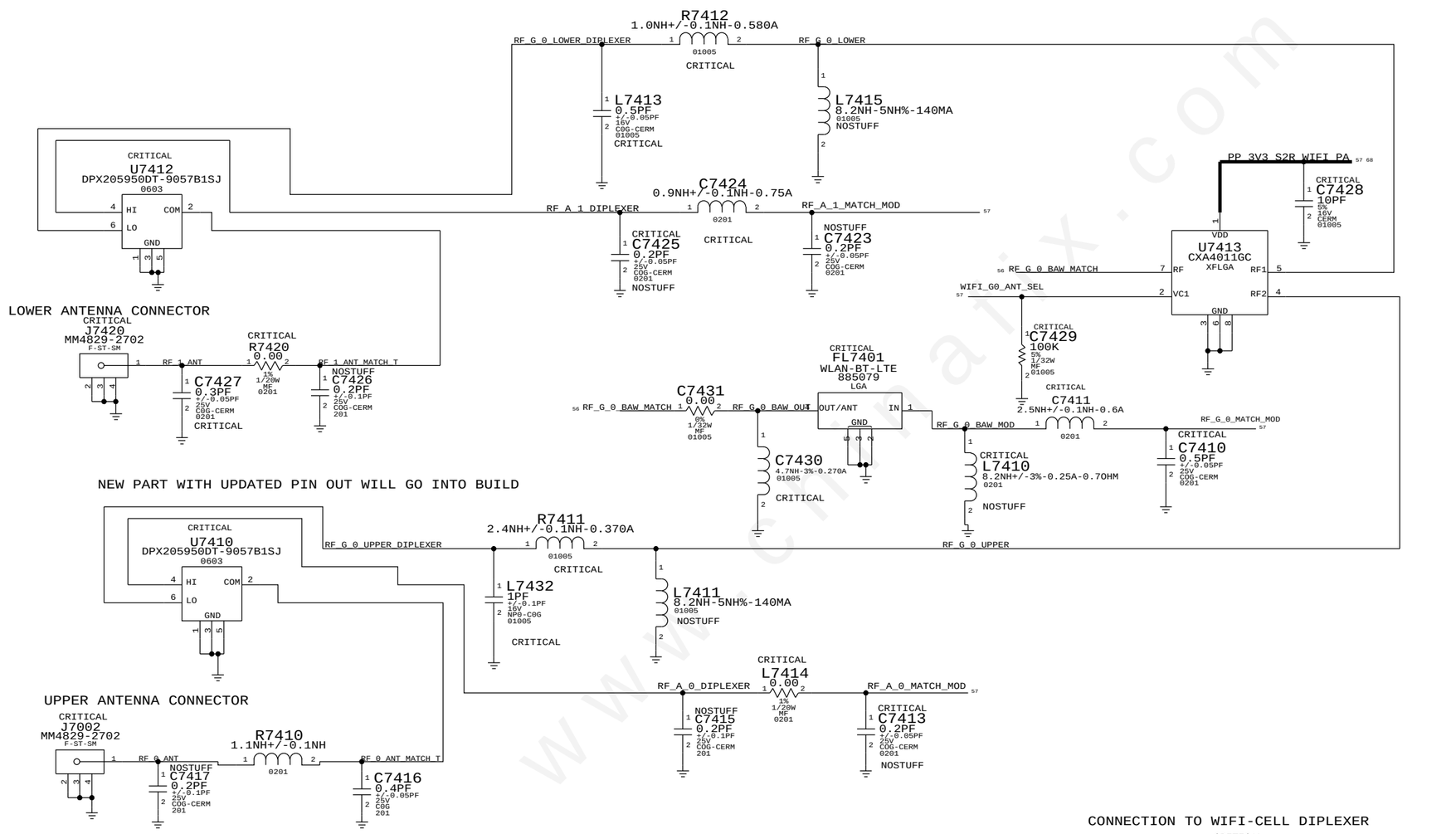
WIFI/BT (2 OF 5)
WIFI/BT FRONT END FOR J82



PAGE TITLE	WIFI/BT: J82 ANT INTERFACE
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DRAWING NUMBER	051-0301
SIZE	D
REVISION	B.0.0
BRANCH	
PAGE	74 OF 155
SHEET	56 OF 73

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WIFI/BT (3 OF 5)

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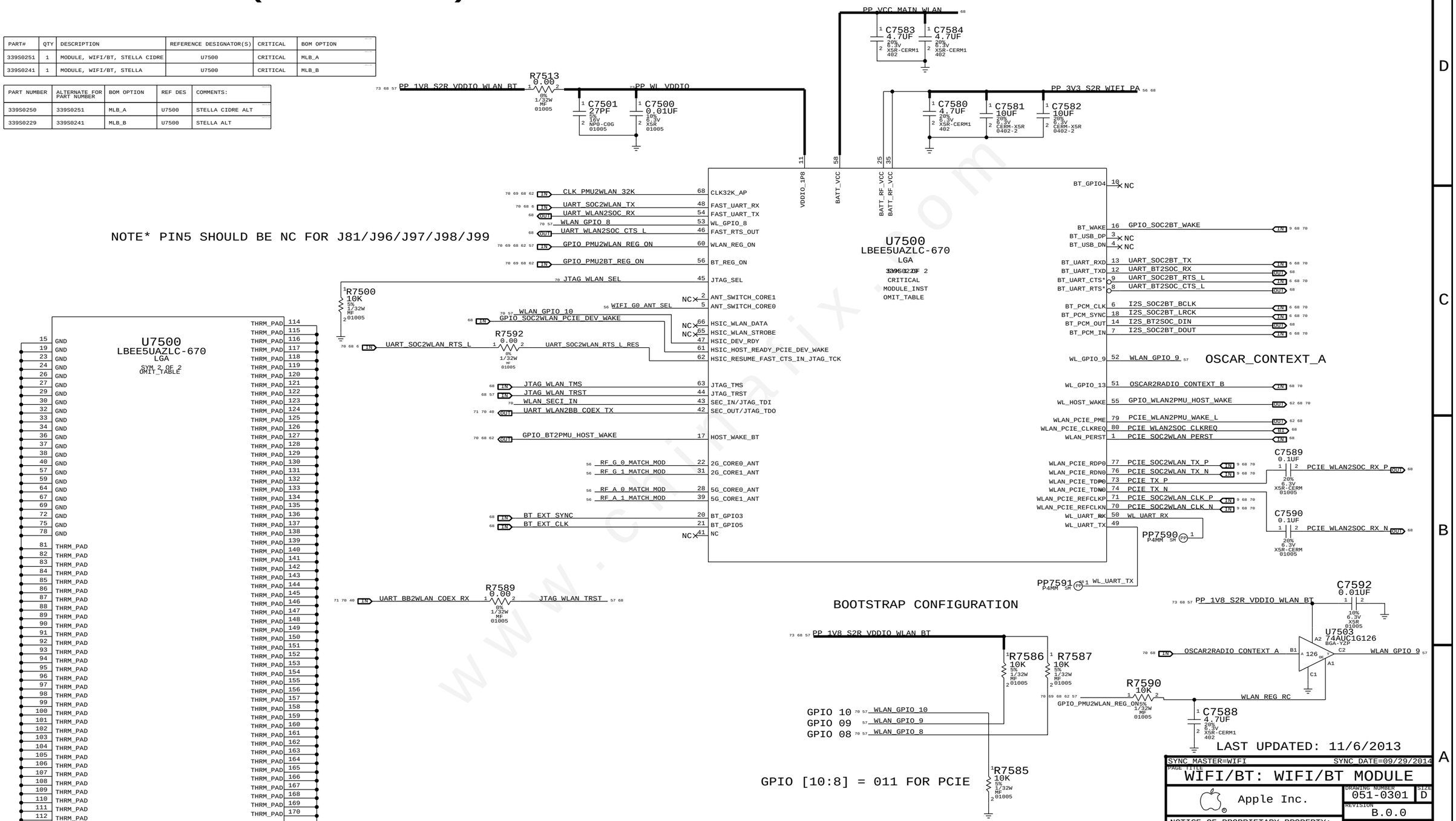
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S0251	1	MODULE, WIFI/BT, STELLA CIDRE	U7500	CRITICAL	MLB_A
339S0241	1	MODULE, WIFI/BT, STELLA	U7500	CRITICAL	MLB_B

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0250	339S0251	MLB_A	U7500	STELLA CIDRE ALT
339S0229	339S0241	MLB_B	U7500	STELLA ALT



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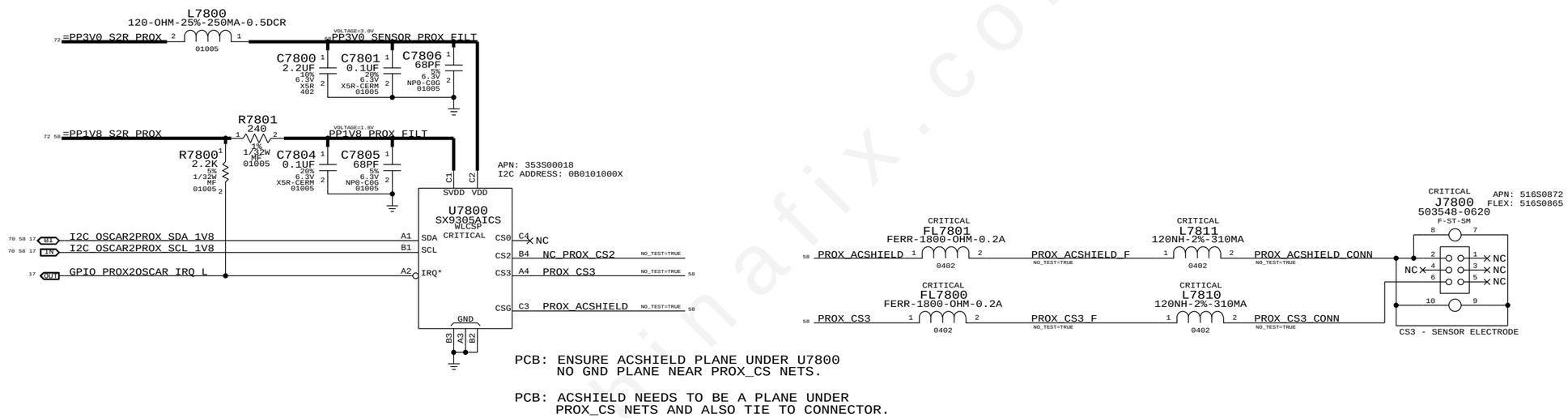
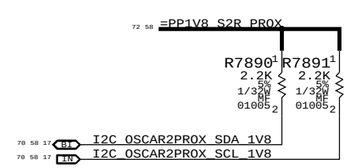


PCB: ENSURE ACSHIELD PLANE UNDER U7800
NO GND PLANE NEAR PROX_CS NETS.

PCB: ACSHIELD NEEDS TO BE A PLANE UNDER
PROX_CS NETS AND ALSO TIE TO CONNECTOR.



SYNC_MASTER=N/A	SYNC_DATE=N/A
PAGE TITLE: SENSOR: HAMMERHEAD	
Apple Inc.	DRAWING NUMBER: 051-0301 SIZE: D
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	PAGE: 78 OF 155
	SHEET: 58 OF 73

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
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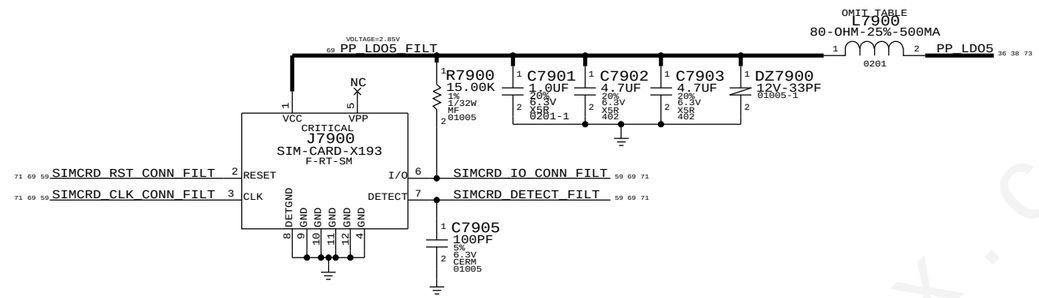
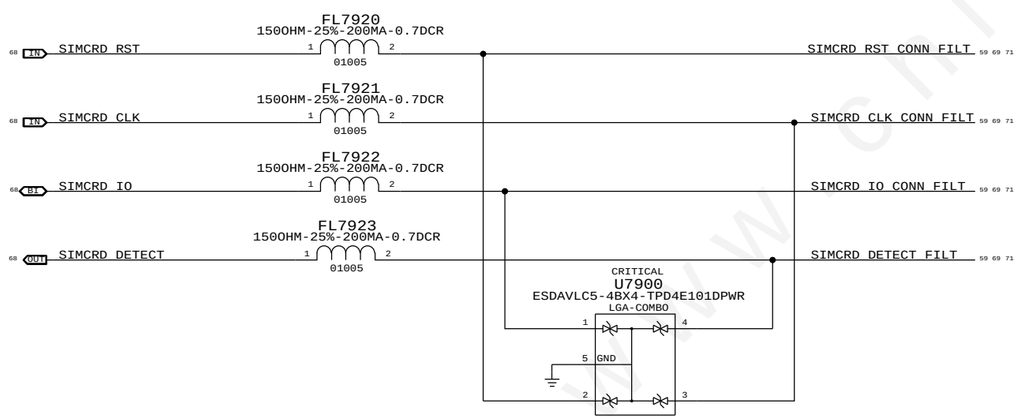
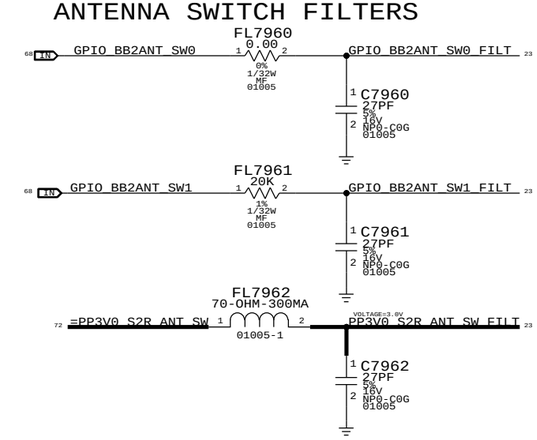
SIM CARD AND ANTENNA SWITCH FILTERS





ANTENNA SWITCH FILTERS



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
CELL: SIM AND ANT SW FILT

Apple Inc.

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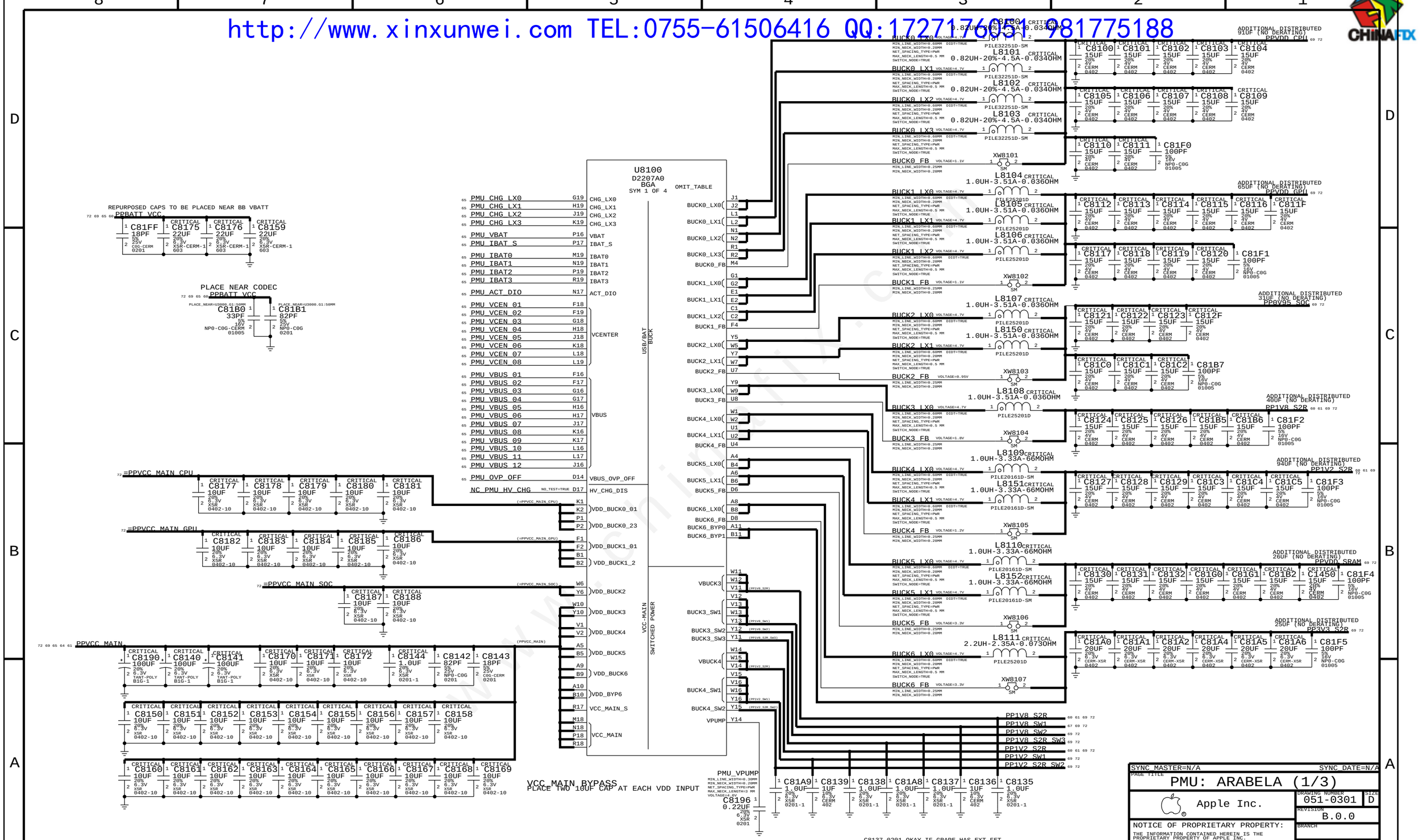

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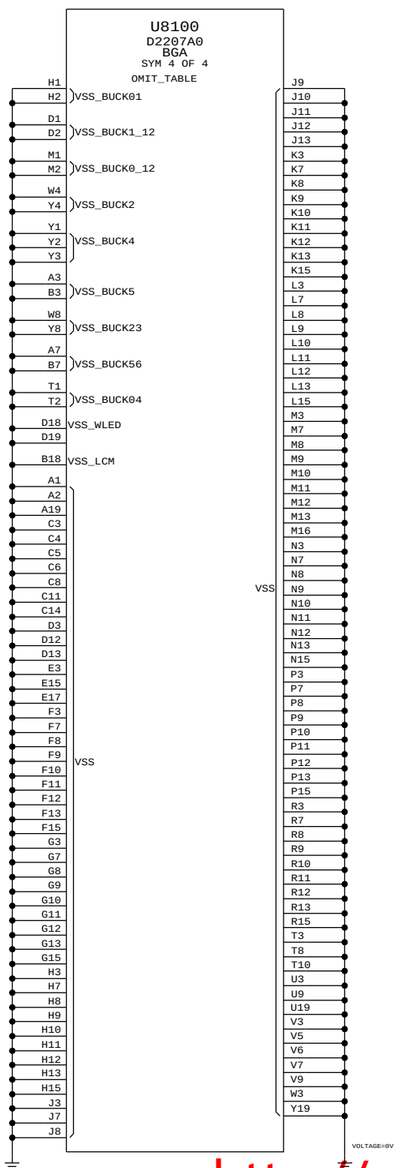
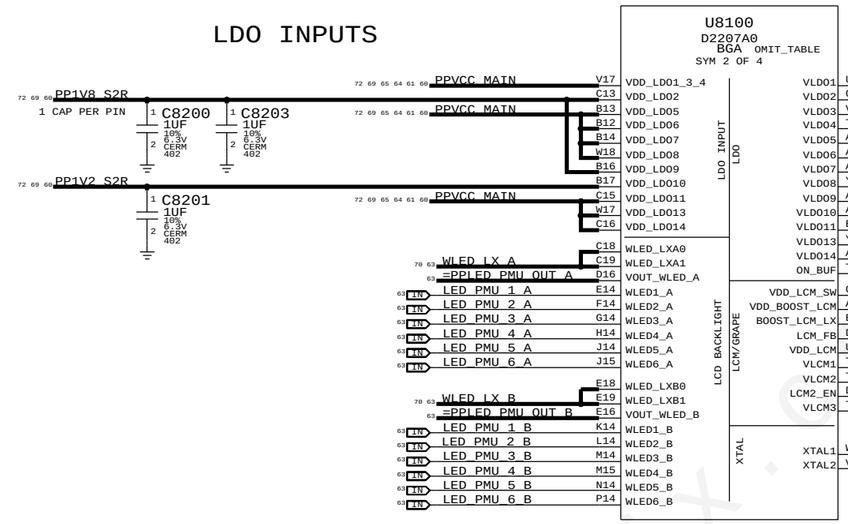
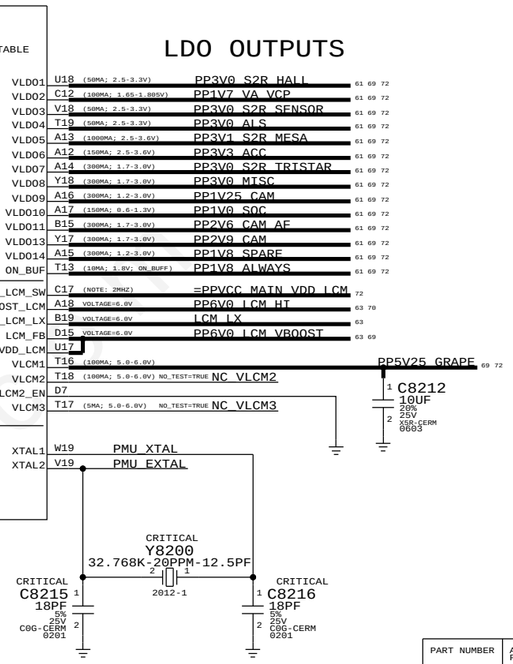
PCB: ADD A VIA PER PIN FOR ALL VSS_* AND VSSA_* PINS



LDO INPUTS

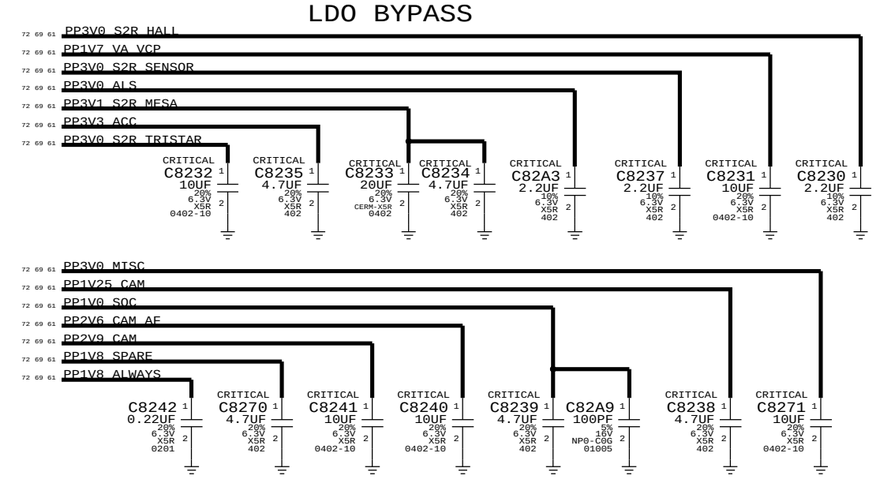


LDO OUTPUTS



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0399	197S0392		Y8200	RDAR://PROBLEM/9936684
138S0703	138S0648		C8235	AND ~15X MORE REFDES

LDO BYPASS



SYNC MASTER=N/A SYNC DATE=N/A

PAGE TITLE
PMU: ARABELA (2/3)

Apple Inc.

DRAWING NUMBER 051-0301 SIZE D

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PAGE 82 OF 155

SHEET 61 OF 73

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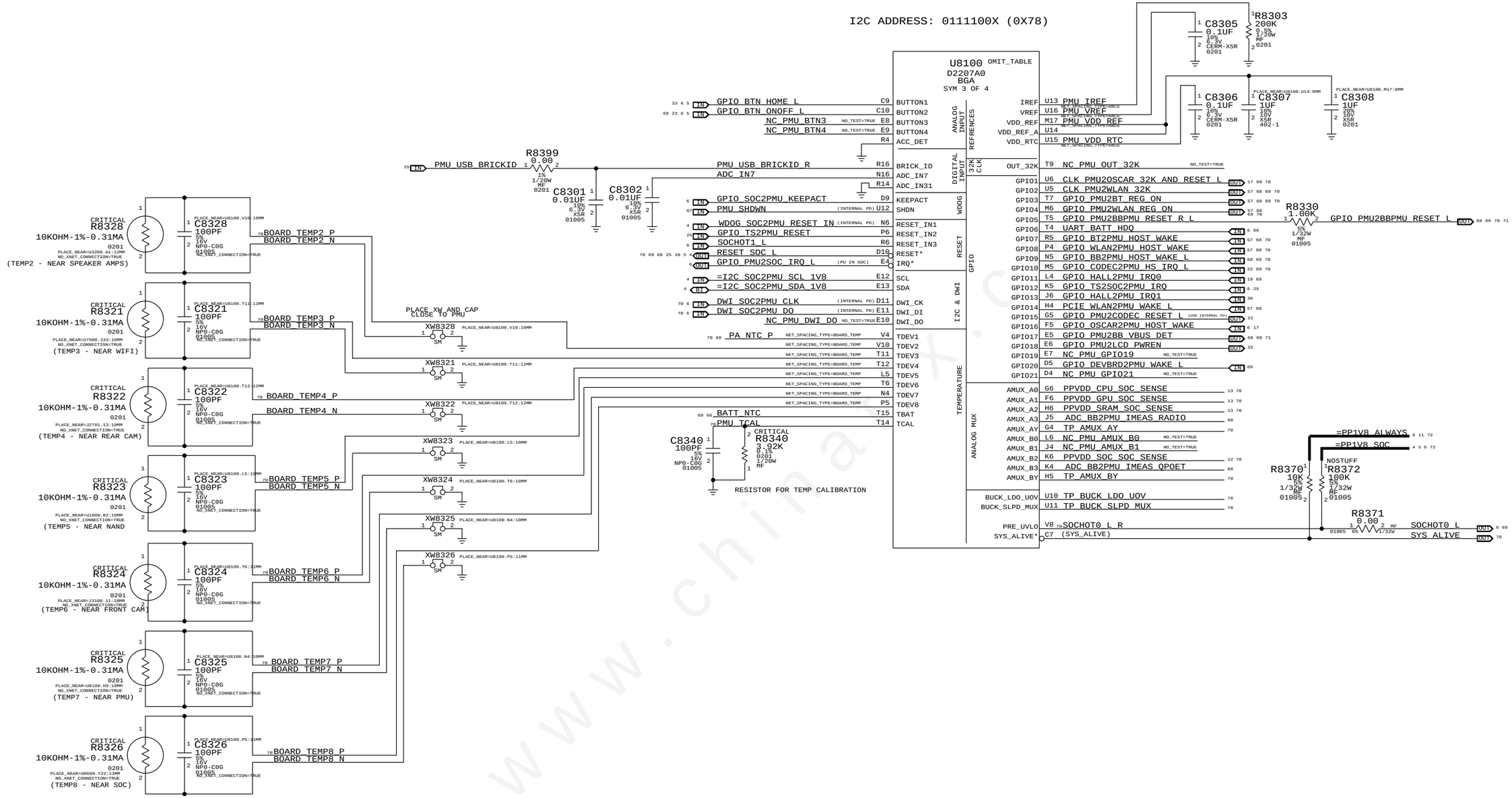

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0706	138S0739		C8308	
118S0764	118S0717		R8340	RDAR://PROBLEM/8380367
107S0150	107S0208		R8321-R8328	RDAR://PROBLEM/8380367

SYNC MASTER=N/A SYNC DATE=N/A

PAGE TITLE
PMU: ARABELA (3/3)

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DRAWING NUMBER 051-0301 SIZE D
REVISION B.0.0
BRANCH
PAGE 83 OF 155
SHEET 62 OF 73

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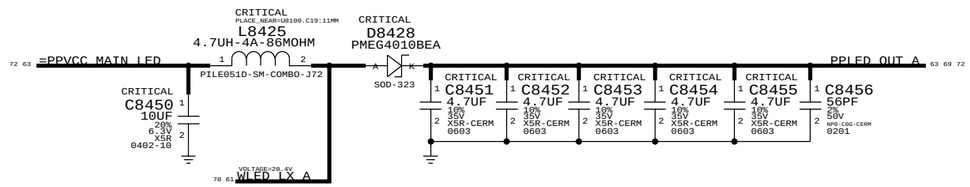
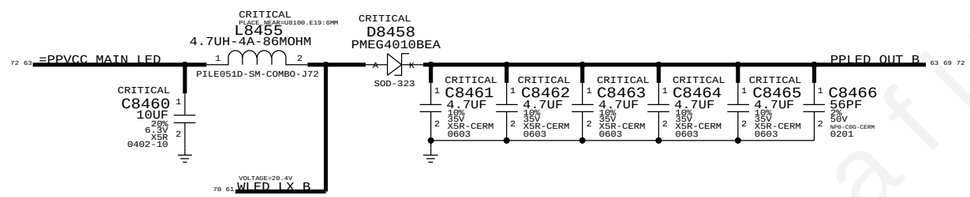
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1837	152S1789		L8425,L8455	RDAR://PROBLEM/13487208

BACKLIGHT CIRCUIT MOVED HERE TO PERMIT SYNCING WITH DESIGNS USING BEACON

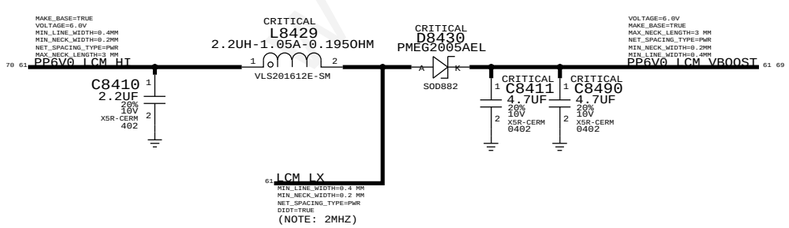


PPLED_OUT_A MAKE_BASE=TRUE — =PPLED_PMU_OUT_A
LED_IO_1_A MAKE_BASE=TRUE — LED_PMU_1_A
LED_IO_2_A MAKE_BASE=TRUE — LED_PMU_2_A
LED_IO_3_A MAKE_BASE=TRUE — LED_PMU_3_A
LED_IO_4_A MAKE_BASE=TRUE — LED_PMU_4_A
LED_IO_5_A MAKE_BASE=TRUE — LED_PMU_5_A
LED_IO_6_A MAKE_BASE=TRUE — LED_PMU_6_A



PPLED_OUT_B MAKE_BASE=TRUE — =PPLED_PMU_OUT_B
LED_IO_1_B MAKE_BASE=TRUE — LED_PMU_1_B
LED_IO_2_B MAKE_BASE=TRUE — LED_PMU_2_B
LED_IO_3_B MAKE_BASE=TRUE — LED_PMU_3_B
LED_IO_4_B MAKE_BASE=TRUE — LED_PMU_4_B
LED_IO_5_B MAKE_BASE=TRUE — LED_PMU_5_B
LED_IO_6_B MAKE_BASE=TRUE — LED_PMU_6_B

LCM BOOST MOVED HERE TO PERMIT SYNCING WITH DESIGNS USING KONA



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
POWER: J82 SPECIFIC

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PAGE 84 OF 155
SHEET 63 OF 73

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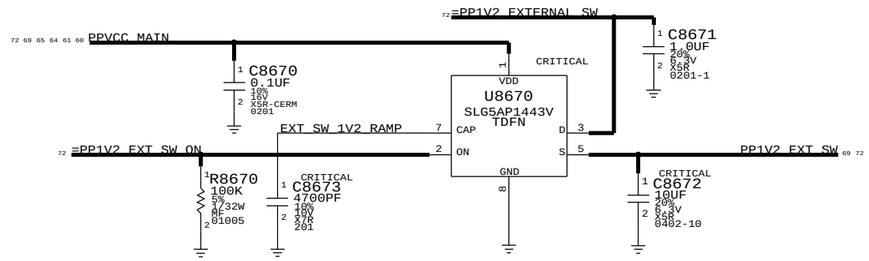
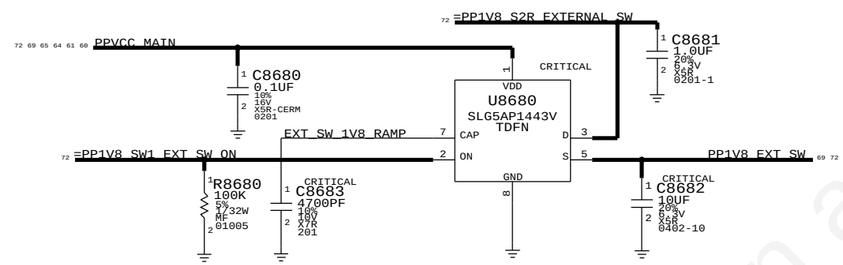
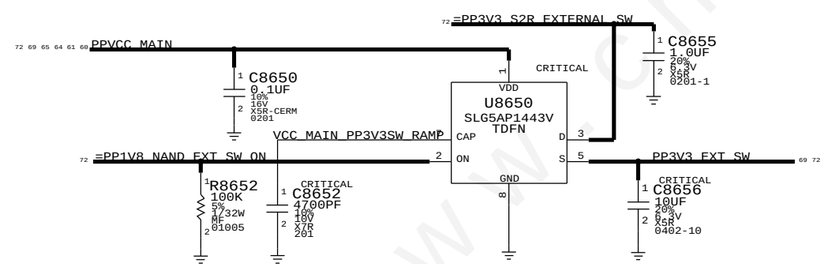




BUCK6 POWER IS ON IN HIBERNATE DUE TO WIFI PAS
SWITCH NEEDED TO GATE POWER TO NAND AND SOC



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SYNC MASTER=N/A SYNC DATE=N/A

PAGE TITLE
POWER: EXTERNAL SWITCHES

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REVISION B.0.0
BRANCH
PAGE 86 OF 155
SHEET 64 OF 73

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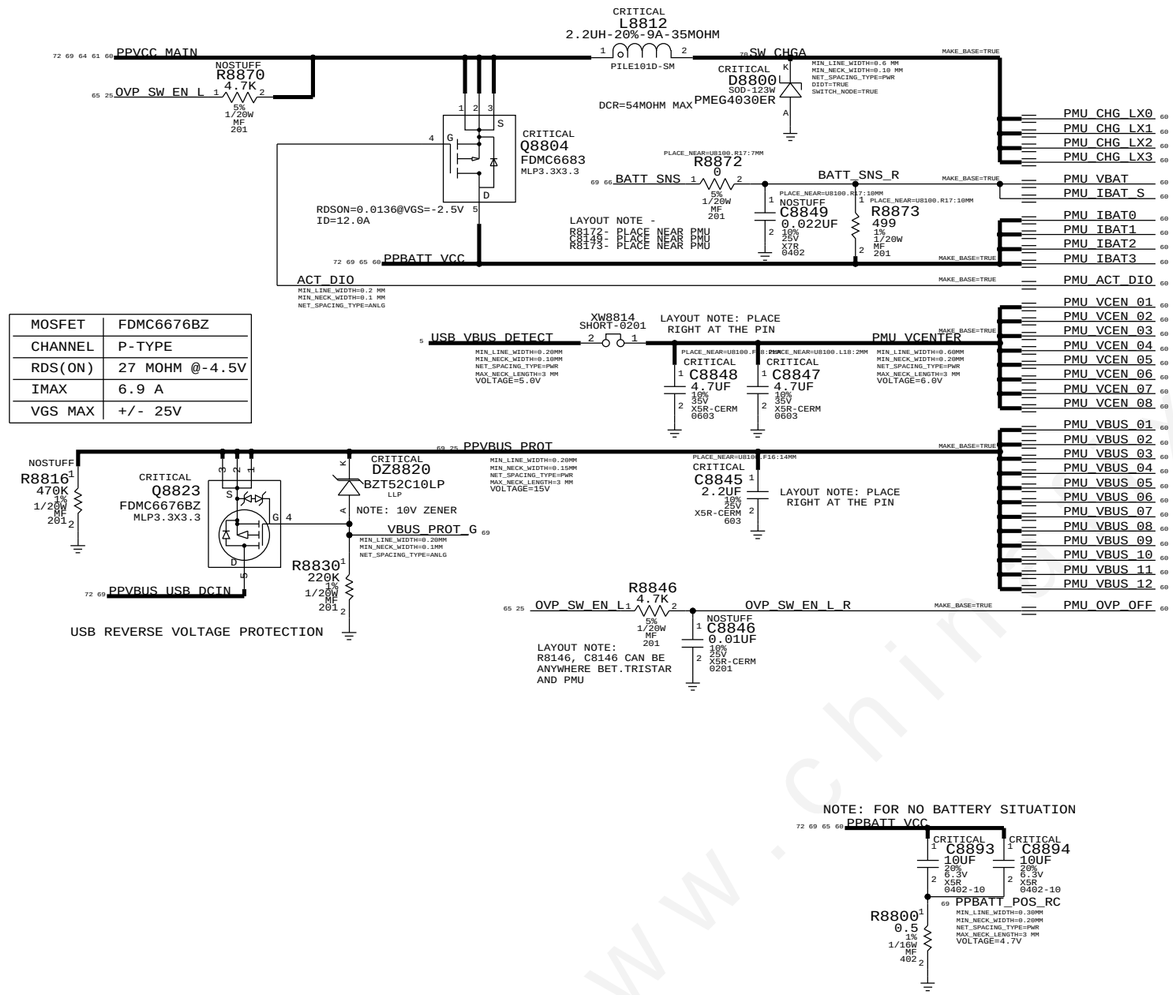
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1192	376S0929	?	Q8823	RDAR://PROBLEM/16073848



MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

SYNC MASTER=N/A SYNC DATE=N/A

PAGE TITLE: PMU: CHARGER BUCK

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REVISION: B.0.0

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PAGE: 88 OF 155

SHEET: 65 OF 73

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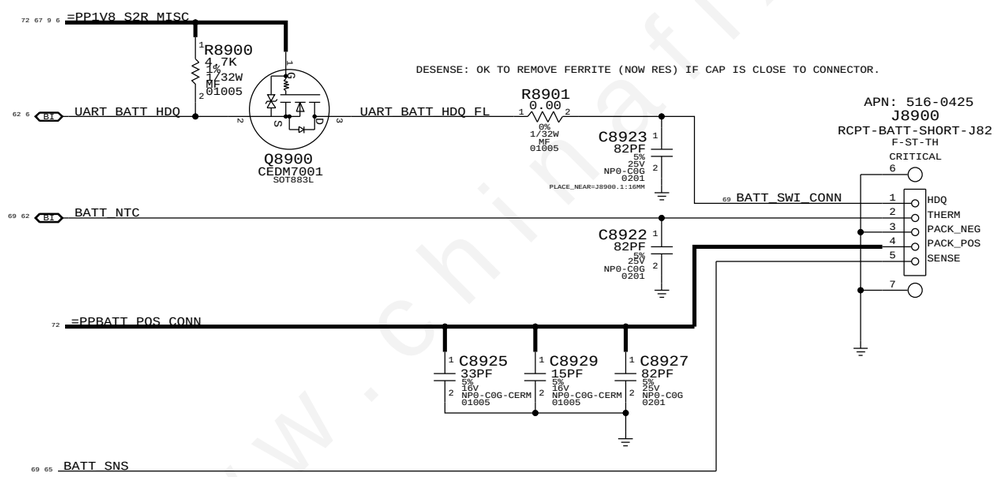

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0644	155S0822		FL8900	BOAR://PROBLEM/41282871

SYNC MASTER=N/A SYNC DATE=N/A

PAGE TITLE
POWER: BATTERY CONN

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PAGE 89 OF 155

SHEET 66 OF 73

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DEBUG RESET ACCESS

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SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: SOC: DEBUG

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PAGE: 90 OF 155

SHEET: 67 OF 73

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CELLULAR AND WLAN/BT ALIASES

BASEBANDGPIO

71 69 6	IN	GPIO_SOC2BB_RADIO_ON_L	MAKE_BASE=TRUE	RADIO_ON_L	OUT 35 37
69 6	IN	GPIO_SOC2BB_RESET_L	MAKE_BASE=TRUE	BB_RST_L	OUT 35 37
69 6	OUT	GPIO_BB2SOC_RESET_DET_L	MAKE_BASE=TRUE	BB_RESET_DET_L	IN 35 40
71 70 69 62	IN	GPIO_PMU2BBPMU_RESET_L	MAKE_BASE=TRUE	RF_PMIC_RESET_L	OUT 35 37
71 6	IN	GPIO_SOC2BB_WAKE_MODEM	MAKE_BASE=TRUE	AP_WAKE_MODEM	OUT 40
70 69 62 25 10 5 4	OUT	RESET_SOC_L	MAKE_BASE=TRUE	RESET_1V8_L	IN 35
71 6	IN	GPIO_SOC2BB_COREDUMP	MAKE_BASE=TRUE	BB_CORE_DUMP	OUT 40
6	BI	GPIO_BB_IPC	MAKE_BASE=TRUE	BB_IPC_GPIO	BI 40
71 6	OUT	GPIO_BB2SOC_GPS_SYNC	MAKE_BASE=TRUE	BB_GPS_SYNC	IN 40
70 69 62	OUT	GPIO_BB2PMU_HOST_WAKE_L	MAKE_BASE=TRUE	BB_WAKE_HOST	IN 35 40

UART

71 25 6	OUT	UART_BB2SOC_TX	MAKE_BASE=TRUE	BB_UART_TXD	IN 35 40
71 25 6	IN	UART_SOC2BB_TX	MAKE_BASE=TRUE	BB_UART_RXD	OUT 35 40
71 6	OUT	UART_BB2SOC_RTS_L	MAKE_BASE=TRUE	BB_UART_RTS_L	IN 40
71 6	IN	UART_SOC2BB_RTS_L	MAKE_BASE=TRUE	BB_UART_CTS_L	OUT 40
71 17	IN	UART_OSCAR2BB_TX	MAKE_BASE=TRUE	BB_OTHER_RXD	OUT 40
71 17	OUT	UART_BB2OSCAR_TX	MAKE_BASE=TRUE	BB_OTHER_TXD	IN 40

HSIC

69 6	IN	HSIC_SOC2BB_HOST_RDY	MAKE_BASE=TRUE	BB_HOST_RDY	OUT 35 40
69 6	OUT	HSIC_BB2SOC_DEVICE_RDY	MAKE_BASE=TRUE	BB_DEVICE_RDY	IN 35 40
71 5	BI	HSIC_BB_DATA	MAKE_BASE=TRUE	50_BB_HSIC_DATA	BI 35 39
71 5	BI	HSIC_BB_STB	MAKE_BASE=TRUE	50_BB_HSIC_STROBE	BI 35 39

USB

71 69 62	IN	GPIO_PMU2BB_VBUS_DET	MAKE_BASE=TRUE	BB_USB_VBUS	OUT 35 39
71 25	BI	USB_BB_P	MAKE_BASE=TRUE	90_BB_USB_P	BI 35
71 25	BI	USB_BB_N	MAKE_BASE=TRUE	90_BB_USB_N	BI 35

SIM CARD

59	IN	SIMCRD_DETECT	MAKE_BASE=TRUE	BB_SIM_DETECT	OUT 39 40
59	OUT	SIMCRD_RST	MAKE_BASE=TRUE	BB_SIM_RESET	IN 40
59	OUT	SIMCRD_CLK	MAKE_BASE=TRUE	BB_SIM_CLK	IN 40
59	BI	SIMCRD_IO	MAKE_BASE=TRUE	BB_SIM_DATA	BI 40

ADC

62	OUT	ADC_BB2PMU_IMEAS_RADIO	MAKE_BASE=TRUE	RADIO_TO_PMU_ADC_IMEAS_RADIO	IN 35
62	OUT	ADC_BB2PMU_IMEAS_QPOET	MAKE_BASE=TRUE	RADIO_TO_PMU_ADC_IMEAS_QPOET	IN 44

POWER

72	=PPBATT_VCC_BB		PP_BATT_VCC	35 44 53 73

LOWER ANT CTRL

59	OUT	GPIO_BB2ANT_SW0	MAKE_BASE=TRUE	BB_ANTSW_GPIO0	IN 40
59	OUT	GPIO_BB2ANT_SW1	MAKE_BASE=TRUE	BB_ANTSW_GPIO1	IN 40

WLAN/BTGPIO

70 69 68 62 57	IN	CLK_PMU2WLAN_32K	MAKE_BASE=TRUE	CLK_PMU2WLAN_32K	OUT 57 62 68 69 70
70 69 68 62 57	IN	GPIO_PMU2BT_REG_ON	MAKE_BASE=TRUE	GPIO_PMU2BT_REG_ON	OUT 57 62 68 69 70
70 69 68 62 57	IN	GPIO_PMU2WLAN_REG_ON	MAKE_BASE=TRUE	GPIO_PMU2WLAN_REG_ON	OUT 57 62 68 69 70
70 68 57 9	IN	GPIO_SOC2BT_WAKE	MAKE_BASE=TRUE	GPIO_SOC2BT_WAKE	OUT 9 57 68 70
70 9	IN	GPIO_SOC2WLAN_WAKE	MAKE_BASE=TRUE	GPIO_SOC2WLAN_PCIE_DEV_WAKE	OUT 57
70 68 62 57	OUT	GPIO_BT2PMU_HOST_WAKE	MAKE_BASE=TRUE	GPIO_BT2PMU_HOST_WAKE	IN 57 62 68 70
70 68 62 57	OUT	GPIO_WLAN2PMU_HOST_WAKE	MAKE_BASE=TRUE	GPIO_WLAN2PMU_HOST_WAKE	IN 57 62 68 70

PCIE

70 9	IN	PCIE_SOC2WLAN_RESET_L	MAKE_BASE=TRUE	PCIE_SOC2WLAN_PERST	OUT 57
70 9	OUT	PCIE_WLAN2SOC_CLKREQ_L	MAKE_BASE=TRUE	PCIE_WLAN2SOC_CLKREQ	IN 57
68 62 57	OUT	PCIE_WLAN2PMU_WAKE_L	MAKE_BASE=TRUE	PCIE_WLAN2PMU_WAKE_L	IN 57 62 68
70 68 57 9	IN	PCIE_SOC2WLAN_CLK_P	MAKE_BASE=TRUE	PCIE_SOC2WLAN_CLK_P	OUT 9 57 68 70
70 68 57 9	IN	PCIE_SOC2WLAN_CLK_N	MAKE_BASE=TRUE	PCIE_SOC2WLAN_CLK_N	OUT 9 57 68 70
70 68 57 9	IN	PCIE_SOC2WLAN_TX_P	MAKE_BASE=TRUE	PCIE_SOC2WLAN_TX_P	OUT 9 57 68 70
70 68 57 9	IN	PCIE_SOC2WLAN_TX_N	MAKE_BASE=TRUE	PCIE_SOC2WLAN_TX_N	OUT 9 57 68 70
70 9	OUT	PCIE_WLAN2SOC_TX_P	MAKE_BASE=TRUE	PCIE_WLAN2SOC_RX_P	IN 57
70 9	OUT	PCIE_WLAN2SOC_TX_N	MAKE_BASE=TRUE	PCIE_WLAN2SOC_RX_N	IN 57
70		PCIE_WLAN2SOC_TX_C_P	MAKE_BASE=TRUE	PCIE_TX_P	57
70		PCIE_WLAN2SOC_TX_C_N	MAKE_BASE=TRUE	PCIE_TX_N	57

TO KEEP PP NAMING CONSISTENT

UART

70 68 57 6	IN	UART_SOC2BT_TX	MAKE_BASE=TRUE	UART_SOC2BT_TX	OUT 6 57 68 70
70 68 57 6	IN	UART_SOC2BT_RTS_L	MAKE_BASE=TRUE	UART_SOC2BT_RTS_L	OUT 6 57 68 70
70 6	OUT	UART_BT2SOC_TX	MAKE_BASE=TRUE	UART_BT2SOC_RX	IN 57
70 6	OUT	UART_BT2SOC_RTS_L	MAKE_BASE=TRUE	UART_BT2SOC_CTS_L	IN 57
70 68 57 6	IN	UART_SOC2WLAN_TX	MAKE_BASE=TRUE	UART_SOC2WLAN_TX	OUT 6 57 68 70
70 68 57 6	IN	UART_SOC2WLAN_RTS_L	MAKE_BASE=TRUE	UART_SOC2WLAN_RTS_L	OUT 6 57 68 70
70 6	OUT	UART_WLAN2SOC_TX	MAKE_BASE=TRUE	UART_WLAN2SOC_RX	IN 57
70 6	OUT	UART_WLAN2SOC_RTS_L	MAKE_BASE=TRUE	UART_WLAN2SOC_CTS_L	IN 57
		TP_WL_UART_RX	MAKE_BASE=TRUE	WL_UART_RX	57
		TP_WL_UART_TX	MAKE_BASE=TRUE	WL_UART_TX	57

RESOLVES CKPLUS ERROR IN NAME

I2S

70 6	OUT	I2S_BT2SOC_DOUT	MAKE_BASE=TRUE	I2S_BT2SOC_DIN	IN 57
70 68 57 6	IN	I2S_SOC2BT_DOUT	MAKE_BASE=TRUE	I2S_SOC2BT_DOUT	OUT 5 57 68 70
70 68 57 6	IN	I2S_SOC2BT_BCLK	MAKE_BASE=TRUE	I2S_SOC2BT_BCLK	OUT 5 57 68 70
70 68 57 6	IN	I2S_SOC2BT_LRCK	MAKE_BASE=TRUE	I2S_SOC2BT_LRCK	OUT 5 57 68 70

OSCAR CONTEXT

17	IN	GPIO_OSCAR2WLAN_CONTEXT_A	MAKE_BASE=TRUE	OSCAR2RADIO_CONTEXT_A	OUT 57 70
17	IN	GPIO_OSCAR2WLAN_CONTEXT_B	MAKE_BASE=TRUE	OSCAR2RADIO_CONTEXT_B	OUT 57 70

JTAG

70	OUT	TP_JTAG_WLAN_TMS	MAKE_BASE=TRUE	JTAG_WLAN_TMS	IN 57
70	OUT	TP_JTAG_WLAN_TRST	MAKE_BASE=TRUE	JTAG_WLAN_TRST	IN 57

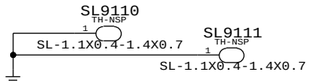
POWER

72	=PPVCC_MAIN_WLAN		PP_VCC_MAIN_WLAN	57
72	=PP3V3_S2R_WIFI_PA		PP_3V3_S2R_WIFI_PA	56 57
72	=PP1V8_S2R_VDDIO_WLAN_BT		PP_1V8_S2R_VDDIO_WLAN_BT	57 73

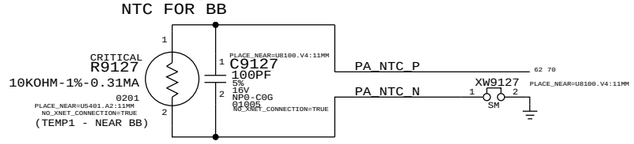
NO CONNECT

	NC_WLAN_GPIO3	NO_TEST=TRUE	MAKE_BASE=TRUE	BT_EXT_SYNC	OUT 57
	NC_WLAN_GPIO5	NO_TEST=TRUE	MAKE_BASE=TRUE	BT_EXT_CLK	OUT 57

SLOTS FOR RADIO FENCE



NTC FOR BB



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: ALIASES: BB/WLAN/BT

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PAGE: 91 OF 155

SHEET: 68 OF 73

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POWER - BUCKS (MUST HAVE)

PPVDD_CPU	FUNC_TEST=TRUE	60 72
PPVDD_GPU	FUNC_TEST=TRUE	60 72
PP0V95_SOC	FUNC_TEST=TRUE	60 72
PP1V8_S2R	FUNC_TEST=TRUE	60 61 72
PP1V8_SW1	FUNC_TEST=TRUE	60 67 72
PP1V8_SW1_FOREHEAD	FUNC_TEST=TRUE	72
PP1V8_EXT_SW	FUNC_TEST=TRUE	64 72
PP1V8_SW2	FUNC_TEST=TRUE	60 72
PP1V8_GRAPE_EXT_SW	FUNC_TEST=TRUE	30 72
PP1V8_S2R_SW3	FUNC_TEST=TRUE	60 72
PP1V2_S2R	FUNC_TEST=TRUE	60 61 72
PP1V2_SW1	FUNC_TEST=TRUE	60 72
PP1V2_EXT_SW	FUNC_TEST=TRUE	64 72
PP1V2_S2R_SW2	FUNC_TEST=TRUE	60 72
PPVDD_SRAM	FUNC_TEST=TRUE	60 72
PP3V3_S2R	FUNC_TEST=TRUE	60 72
PP3V3_EXT_SW	FUNC_TEST=TRUE	64 72

POWER - LDOS

PP1V7_VA_VCP	FUNC_TEST=TRUE	61 72
PP3V0_S2R_SENSOR	FUNC_TEST=TRUE	61 72
PP3V0_ALS	FUNC_TEST=TRUE	61 72
PP3V3_ACC	FUNC_TEST=TRUE	61 72
PP3V0_S2R_TRISTAR	FUNC_TEST=TRUE	61 72
PP3V1_S2R_MESA	FUNC_TEST=TRUE	61 72
PP1V0_SOC	FUNC_TEST=TRUE	61 72
PP1V8_SPARE	FUNC_TEST=TRUE	61 72
PP3V0_S2R_HALL	FUNC_TEST=TRUE	61 72
PP3V0_MISC	FUNC_TEST=TRUE	61 72
PP1V25_CAM	FUNC_TEST=TRUE	61 72
PP2V6_CAM_AF	FUNC_TEST=TRUE	61 72
PP2V9_CAM	FUNC_TEST=TRUE	61 72

POWER - OTHER (MUST HAVE)

PP1V8_ALWAYS	FUNC_TEST=TRUE	61 72
PPBATT_VCC	FUNC_TEST=TRUE	60 65 69 72
PPLED_OUT_A	FUNC_TEST=TRUE	63 72
PPLED_OUT_B	FUNC_TEST=TRUE	63 72
PP5V25_GRAPE	FUNC_TEST=TRUE	61 72
PP1V8_XTAL	FUNC_TEST=TRUE	11
PPVCC_MAIN	FUNC_TEST=TRUE	60 61 64 65 72
PPBATT_POS_RC	FUNC_TEST=TRUE	65
PP6V0_LCM_VBOOST	FUNC_TEST=TRUE	61 63
PPVBUS_USB_DCIN	FUNC_TEST=TRUE	65 72
PPVBUS_PROT	FUNC_TEST=TRUE	25 65
VBUS_PROT_G	FUNC_TEST=TRUE	65

POWER - CAMERA (FRONT) (MUST HAVE)

PP1V2_CAM_FRONT_FILT	FUNC_TEST=TRUE	20 21
PP1V8_CAM_FRONT_FILT	FUNC_TEST=TRUE	20 21
PP2V9_AVDD_CAM_FRONT_FILT	FUNC_TEST=TRUE	20 21

POWER - CAMERA (REAR)

PP1V25_CAM_REAR_FILT	FUNC_TEST=TRUE	20 21
PP1V8_CAM_REAR_FILT	FUNC_TEST=TRUE	20 21
PP2V6_CAM_REAR_AF_FILT	FUNC_TEST=TRUE	20 21
PP2V9_AVDD_CAM_REAR_FILT	FUNC_TEST=TRUE	20 21

POWER - AUDIO

PP1V8_DMIC_MIC_FILT	FUNC_TEST=TRUE	23
PP1V8_DMIC_BTN_FILT	FUNC_TEST=TRUE	28
PP1V7_VCP	FUNC_TEST=TRUE	22
PPVBOOST_R	FUNC_TEST=TRUE	24
PPVBOOST_L	FUNC_TEST=TRUE	24

POWER - SENSORS

PP1V8_COMPASS	FUNC_TEST=TRUE	18
PP1V8_PHOS_FILT	FUNC_TEST=TRUE	18
PP1V8_OSCAR_FILT	FUNC_TEST=TRUE	17
PP1V2_OSCAR_FILT	FUNC_TEST=TRUE	17
PP3V0_GYRO_FILT	FUNC_TEST=TRUE	18
PP3V0_SENSOR_PROX_FILT	FUNC_TEST=TRUE	58

POWER - DISPLAY (MUST HAVE)

PPVCC_MAIN_LCD_SW_CONN	FUNC_TEST=TRUE	31 32
PPVCC_MAIN_LCD_SW	FUNC_TEST=TRUE	32

POWER - MESA (MUST HAVE)

PP1V825_S2R_MESA_FILT	FUNC_TEST=TRUE	31 33
PP3V1_S2R_MESA_FILT	FUNC_TEST=TRUE	31 33
PP11V3_MESA_FILT	FUNC_TEST=TRUE	31 33

POWER - GRAPE

PPVDD_STINGER_BOOST	FUNC_TEST=TRUE	29

POWER - BACKLIGHT (MUST HAVE)

PPLED_BACK_REG_A	FUNC_TEST=TRUE	31 32
LED_IO_1_A	FUNC_TEST=TRUE	31 63
LED_IO_2_A	FUNC_TEST=TRUE	31 63
LED_IO_3_A	FUNC_TEST=TRUE	31 63
LED_IO_4_A	FUNC_TEST=TRUE	31 63
LED_IO_5_A	FUNC_TEST=TRUE	31 63
LED_IO_6_A	FUNC_TEST=TRUE	31 63
PPLED_BACK_REG_B	FUNC_TEST=TRUE	31 32
LED_IO_1_B	FUNC_TEST=TRUE	31 63
LED_IO_2_B	FUNC_TEST=TRUE	31 63
LED_IO_3_B	FUNC_TEST=TRUE	31 63
LED_IO_4_B	FUNC_TEST=TRUE	31 63
LED_IO_5_B	FUNC_TEST=TRUE	31 63
LED_IO_6_B	FUNC_TEST=TRUE	31 63

SOC - JTAG/RESET (MUST HAVE)

JTAG_SOC_SEL	FUNC_TEST=TRUE	4 5
JTAG_SOC_TCK	FUNC_TEST=TRUE	5 25
JTAG_SOC_TDI	FUNC_TEST=TRUE	5
JTAG_SOC_TMS	FUNC_TEST=TRUE	5 25
TP_JTAG_SOC_TRST_L	FUNC_TEST=TRUE	4 5
TP_JTAG_SOC_TDO	FUNC_TEST=TRUE	5
SOC_TESTMODE	FUNC_TEST=TRUE	4 5
RESET_SOC_L	FUNC_TEST=TRUE	4 5 10 25 62 68 70
GPIO_FORCE_DFU	FUNC_TEST=TRUE	6 67

SOC - UART

UART_SOC2DEBUG_TX	FUNC_TEST=TRUE	6 25
UART_DEBUG2SOC_TX	FUNC_TEST=TRUE	6 25

SOC - USB

USB_SOC_N	FUNC_TEST=TRUE	5 25
USB_SOC_P	FUNC_TEST=TRUE	5 25

E75

E75_ACC_DET_CONN_L	FUNC_TEST=TRUE	25 27
PPVBUS_E75_USB_CONN	FUNC_TEST=TRUE	26 27 69
PPOUT_E75_ACC_ID1_CONN	FUNC_TEST=TRUE	26 27
PPOUT_E75_ACC_ID2_CONN	FUNC_TEST=TRUE	26 27
E75_DPAIR1_CONN_N	FUNC_TEST=TRUE	25 27
E75_DPAIR1_CONN_P	FUNC_TEST=TRUE	25 27
E75_DPAIR2_CONN_N	FUNC_TEST=TRUE	25 27
E75_DPAIR2_CONN_P	FUNC_TEST=TRUE	25 27

AUDIO - HEADPHONE (MUST HAVE)

CONN_HP_HEADSET_DET_FILT	FUNC_TEST=TRUE	22 23
CONN_HP_HS3_FILT	FUNC_TEST=TRUE	22 23
CONN_HP_HS3_REF_FILT	FUNC_TEST=TRUE	22 23
CONN_HP_HS4_FILT	FUNC_TEST=TRUE	22 23
CONN_HP_HS4_REF_FILT	FUNC_TEST=TRUE	22 23
CONN_HP_LEFT_FILT	FUNC_TEST=TRUE	22 23
CONN_HP_RIGHT_FILT	FUNC_TEST=TRUE	22 23
GPIO_SOC2AJ_HS3_SHUNT_EN_FILT	FUNC_TEST=TRUE	23
GPIO_SOC2AJ_HS4_SHUNT_EN_FILT	FUNC_TEST=TRUE	23

AUDIO - SPEAKER AMPS

SPKRAMP_L_OUT_N	FUNC_TEST=TRUE	24 27 70
SPKRAMP_L_OUT_P	FUNC_TEST=TRUE	24 27 70
SPKRAMP_R_OUT_N	FUNC_TEST=TRUE	24 27 70
SPKRAMP_R_OUT_P	FUNC_TEST=TRUE	24 27 70

AUDIO - CODEC

AIN3P	FUNC_TEST=TRUE	22
AIN3N	FUNC_TEST=TRUE	22
GPIO_CODEC2PMU_HS_IRQ_L	FUNC_TEST=TRUE	22 62 70
GND_AUDIO_CODEC	FUNC_TEST=TRUE	22
MIKEY_TS_P	FUNC_TEST=TRUE	22 25
MIKEY_TS_N	FUNC_TEST=TRUE	22 25

AUDIO - DIGITAL MICS

DMIC_MIC_SCLK	FUNC_TEST=TRUE	22 23
DMIC_BTN_SCLK	FUNC_TEST=TRUE	22 28

BUTTONS

GPIO_BTN_HOME_CONN_L	FUNC_TEST=TRUE	31 33
GPIO_BTN_ONOFF_L	FUNC_TEST=TRUE	5 6 23 62
GPIO_BTN_VOL_UP_L_FILT	FUNC_TEST=TRUE	28
GPIO_BTN_VOL_DOWN_L_FILT	FUNC_TEST=TRUE	28

NAND

ANC0_CE0_L	FUNC_TEST=TRUE	7 16 70
ANC1_CE0_L	FUNC_TEST=TRUE	7 16 70

BATTERY (MUST HAVE)

BATT_SWI_CONN	FUNC_TEST=TRUE	66
BATT_NTC	FUNC_TEST=TRUE	62 66
BATT_SNS	FUNC_TEST=TRUE	65 66

GRAPE

CLK_SOC2GRAPE_32K	FUNC_TEST=TRUE	9 30 70

BASEBAND (MUST HAVE)

BOUNDARY_SCAN_EN	FUNC_TEST=TRUE	35 39
GPIO_PMU2BBPMU_RESET_L	FUNC_TEST=TRUE	62 68 70 71
GPIO_SOC2BB_RADIO_ON_L	FUNC_TEST=TRUE	6 68 71
HSIC_SOC2BB_HOST_RDY	FUNC_TEST=TRUE	6 68
GPIO_BB2SOC_RESET_DET_L	FUNC_TEST=TRUE	6 68
HSIC_BB2SOC_DEVICE_RDY	FUNC_TEST=TRUE	6 68
GPIO_SOC2BB_RESET_L	FUNC_TEST=TRUE	6 68
GPIO_PMU2BB_VBUS_DET	FUNC_TEST=TRUE	62 68 71
GPIO_BB2PMU_HOST_WAKE_L	FUNC_TEST=TRUE	62 68 70

BASEBAND - POWER

PP_LDO6	FUNC_TEST=TRUE	35 36 71 73
PP_LDO13	FUNC_TEST=TRUE	36 38 55 73
VREG_SMPS1_0V90	FUNC_TEST=TRUE	36 38
VREG_SMPS3_0V95	FUNC_TEST=TRUE	36 73

BASEBAND - SIM CARD (MUST HAVE)

PP_LDO5_FILT	FUNC_TEST=TRUE	59
SIMCRD_RST_CONN_FILT	FUNC_TEST=TRUE	59 71
SIMCRD_CLK_CONN_FILT	FUNC_TEST=TRUE	59 71
SIMCRD_IO_CONN_FILT	FUNC_TEST=TRUE	59 71
SIMCRD_DETECT_FILT	FUNC_TEST=TRUE	59 71

WIFI/BT

GPIO_PMU2BT_REG_ON	FUNC_TEST=TRUE	57 62 68 70
GPIO_PMU2WLAN_REG_ON	FUNC_TEST=TRUE	57 62 68 70
CLK_PMU2WLAN_32K	FUNC_TEST=TRUE	57 62 68 70

CAMERA - REAR

ISP_CAM_REAR_CLK_F	FUNC_TEST=TRUE	20 21
ISP_CAM_REAR_SCL_F	FUNC_TEST=TRUE	20 21
ISP_CAM_REAR_SDA_F	FUNC_TEST=TRUE	20 21
ISP_CAM_REAR_SHUTDOWN_L_F	FUNC_TEST=TRUE	20 21

CAMERA - FRONT

ISP_CAM_FRONT_CLK_F	FUNC_TEST=TRUE	20 21
ISP_CAM_FRONT_SCL_F	FUNC_TEST=TRUE	20 21
ISP_CAM_FRONT_SDA_F	FUNC_TEST=TRUE	20 21
ISP_CAM_FRONT_SHUTDOWN_L_F	FUNC_TEST=TRUE	20 21

MESA (MUST HAVE)

GPIO_MESA2SOC_IRQ_FILT	FUNC_TEST=TRUE	31 33
MESA_BOOST_ENABLE_FILT	FUNC_TEST=TRUE	31 33
SPI_MESA_MISO_FILT	FUNC_TEST=TRUE	31 33
SPI_MESA_MOSI_FILT	FUNC_TEST=TRUE	31 33
SPI_MESA_SCLK_FILT	FUNC_TEST=TRUE	31 33

HALL EFFECT (MUST HAVE)

GPIO_HALL2PMU_IRQ0	FUNC_TEST=TRUE	19 62
GPIO_HALL2PMU_IRQ1_FILT	FUNC_TEST=TRUE	29 30
PP3V0_S2R_GRAPE_HALL_FILT	FUNC_TEST=TRUE	29 30

ALS

PP3V0_MIC_ALS_FILT	FUNC_TEST=TRUE	23
PP3V0_HP_ALS_FILT	FUNC_TEST=TRUE	23
GPIO_HP_ALS2SOC_IRQ_L_FILT	FUNC_TEST=TRUE	23
GPIO_MIC_ALS2SOC_IRQ_L_F	FUNC_TEST=TRUE	23
I2C_HP_ALS_SCL_1V8_FILT	FUNC_TEST=TRUE	23 70
I2C_HP_ALS_SDA_1V8_FILT	FUNC_TEST=TRUE	23 70
I2C_MIC_ALS_SCL_1V8_F	FUNC_TEST=TRUE	23 70
I2C_MIC_ALS_SDA_1V8_F	FUNC_TEST=TRUE	23 70

DISPLAY (MUST HAVE)

EDP_HPD_EMI	FUNC_TEST=TRUE	32

OSCAR (MUST HAVE)

CLK_PMU2OSCAR_32K_AND_RESET_L	FUNC_TEST=TRUE	17 62 70

SOCHOT0_L	FUNC_TEST=TRUE	6 62

PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM

SL9300 TH-NSP APN: 998-2691 — SL-1.1X0.4-1.4X0.7
SL9301 TH-NSP — SL-1.1X0.4-1.4X0.7
SL9302 TH-NSP — SL-1.1X0.4-1.4X0.7
SL9320 TH-NSP — SL-1.1X0.4-1.4X0.7
SL9321 TH-NSP — SL-1.1X0.4-1.4X0.7

FOREHEAD B2B STANDOFFS

STD9300 APN: 860-8373 STDOFF-3.3X1.8R1.05H-SM

C9301 0.01UF 10% 6.3V X5R 01005 — STD9301 AC R — STD9301 APN: 860-8373 STDOFF-3.3X1.8R1.05H-SM

09/17/13 AC CAP RDAR://PROBLEM//14999426

STD9303 APN: 860-00013 STDOFF-3.3X1.8R0.84H-TH

BUTTON FLEX B2B STANDOFFS

STD9302 APN: 860-8373 STDOFF-3.3X1.8R1.05H-SM

GRAPE AND DISPLAY B2B STANDOFFS

STD9305 APN: 860-8373 STDOFF-3.3X1.8R1.05H-SM
STD9306 STDOFF-3.3X1.8R1.05H-SM
STD9307 STDOFF-3.3X1.8R1.05H-SM

FID9300 FID 0P5SM1P0SQ-NSP
FID9301 FID 0P5SM1P0SQ-NSP
FID9302 FID 0P5SM1P0SQ-NSP
FID9303 FID 0P5SM1P0SQ-NSP
FID9304 FID 0P5SM1P0SQ-NSP
FID9305 FID 0P5SM1P0SQ-NSP

TP9310A TP-1P0-TOP — PLACE_NEAR=J3700.9:20MM
TP9311A TP-1P0-TOP — PLACE_NEAR=J3700.9:20MM
TP9312A TP-1P0-TOP — PLACE_NEAR=J3700.9:20MM — PPVBUS_E75_USB_CONN 26 27 69
TP9315A TP-1P0-TOP — PLACE_NEAR=J3700.9:30MM
TP9316A TP-1P0-TOP — PLACE_NEAR=J3700.9:30MM
TP9317A TP-1P0-TOP — PLACE_NEAR=J3700.9:30MM

TP9300A TP-1P0-TOP — PLACE_NEAR=J8900.4:20MM
TP9301A TP-1P0-TOP — PLACE_NEAR=J8900.4:20MM
TP9302A TP-1P0-TOP — PLACE_NEAR=J8900.4:20MM — PPBATT_VCC 60 65 69 72
TP9305A TP-1P0-TOP — PLACE_NEAR=J8900.3:20MM
TP9306A TP-1P0-TOP — PLACE_NEAR=J8900.3:20MM
TP9307A TP-1P0-TOP — PLACE_NEAR=J8900.3:20MM

DEV BOARD NET TERMINATION

NC_SOC_GPIO09	NO_TEST=TRUE	MAKE_BASE=TRUE	GPIO_ALS2SOC_DEVBRD_IRQ_L	6
NC_PMU_GPIO20	NO_TEST=TRUE	MAKE_BASE=TRUE	GPIO_DEVBRD2PMU_WAKE_L	62
NC_ULPI_STP	NO_TEST=TRUE	MAKE_BASE=TRUE	GPIO_SOC2DEVBRD_S3E_WAKE	9
NC_ULPI_DATA3	NO_TEST=TRUE	MAKE_BASE=TRUE	GPIO_SOC2DEVBRD_S3E_RESET2_L	9
NC_PCIE_CLKREQ2	NO_TEST=TRUE	MAKE_BASE=TRUE	PCIE_DEVBRD2SOC_CLKREQ_L	9
NC_PCIE_PERST2	NO_TEST=TRUE	MAKE_BASE=TRUE	PCIE_SOC2DEVBRD_RESET_L	9
NC_NAND_SYS_CLK	NO_TEST=TRUE	MAKE_BASE=TRUE	CLK_SOC2DEVBRD_PCIE_24MHZ	9
NC_I2S4_MCK	NO_TEST=TRUE	MAKE_BASE=TRUE	GPIO_DISPLAY_ID0	7
NC_I2S1_MCK	NO_TEST=TRUE	MAKE_BASE=TRUE	GPIO_DISPLAY_ID1	7

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: TEST: TPS/HOLES/FIDUCUALS

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DRAWING NUMBER 051-0301 SIZE D
REVISION B.0.0
BRANCH
PAGE 93 OF 155
SHEET 69 OF 73

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EE CHARACTERIZATION TP

SOC

PP9501 1 RESET SOC L — PLACE_SIDE=TOP — 4 5 10 25 62 68 69
PP9503 1 SOCHOT0 L R — 62
TP GPIO DFU STATUS — FUNC_TEST=TRUE — 6
PP9502 1 TP ANALOGMUXOUT — 5

PP9507 1 PPVDD_CPU_SOC_SENSE — PLACE_NEAR=U0600.AB13:1.5MM — 13 62
PP9508 1 PPVDD_GPU_SOC_SENSE — PLACE_NEAR=U0600.N26:1.5MM — 13 62
PP9509 1 PPVDD_SRAM_SOC_SENSE — PLACE_NEAR=U0600.N25:1.5MM — 13 62
PP9513 1 PPVDD_SOC_SOC_SENSE — PLACE_NEAR=U0600.M25:1.5MM — 12 62

PP9509 1 TP_SOC_VSS_SENSE — PLACE_NEAR=U0600.M26:1MM — 12
PP9510 1 TP_SOC_VSS_CPU_SENSE — PLACE_NEAR=U0600.AC13:1MM — 12

NAND

ANC0 AD<1..7> — FUNC_TEST=TRUE — 7 16
ANC0 CE0 L — FUNC_TEST=TRUE — 7 16 69
ANC0 ALE — FUNC_TEST=TRUE — 7 16
ANC0 CLE — FUNC_TEST=TRUE — 7 16
ANC0 WE L — FUNC_TEST=TRUE — 7 16
ANC0 RE L — FUNC_TEST=TRUE — 7 16

ANC1 AD<0> — FUNC_TEST=TRUE — 7 16
ANC1 CE0 L — FUNC_TEST=TRUE — 7 16 69
ANC1 ALE — FUNC_TEST=TRUE — 7 16
ANC1 CLE — FUNC_TEST=TRUE — 7 16
ANC1 WE L — FUNC_TEST=TRUE — 7 16
ANC1 RE L — FUNC_TEST=TRUE — 7 16
ANC1 DQS — FUNC_TEST=TRUE — 7 16

PPVREF_ANC_SOC — FUNC_TEST=TRUE — 7
PPVREF_ANC_NAND — FUNC_TEST=TRUE — 16
NAND_SLOT0_RDYBSY_L — FUNC_TEST=TRUE — 16

PP9505 1 ANC0 AD<0> — PLACE_SIDE=BOTTOM, PLACE_NEAR=U0600.A37:2MM — 7 16
PP9506 1 ANC0 DQS — NO_XNET_CONNECTION=TRUE, PLACE_SIDE=BOTTOM, PLACE_NEAR=U0600.C36:2MM — 7 16
PP9500 1 GND — NO_XNET_CONNECTION=TRUE, (PLACE_SIDE=TOP)
PP9504 1 =PP1V8_NAND — (PLACE_SIDE=TOP) — 16 72
PP95G0 1 TP_ANC_TCKC_NAND — (PLACE_SIDE=TOP) — 16
PP95G4 1 TP_ANC_TMSC_NAND — (PLACE_SIDE=TOP) — 16

PMU

GPIO_PMU2BBPMU_RESET_L — FUNC_TEST=TRUE — 52 68 69 71
GPIO_BT2PMU_HOST_WAKE — FUNC_TEST=TRUE — 57 62 68 70
GPIO_BB2PMU_HOST_WAKE_L — FUNC_TEST=TRUE — 52 68 69
GPIO_CODEC2PMU_HS_IRQ_L — FUNC_TEST=TRUE — 22 62 69
PMU_TCAL — FUNC_TEST=TRUE — 62
CLK_PMU2WLAN_32K — FUNC_TEST=TRUE — 57 62 68 69 70
CLK_PMU2OSCAR_32K_AND_RESET — FUNC_TEST=TRUE — 17 62 69
PA_NTC_P — FUNC_TEST=TRUE — 52 68
BOARD_TEMP2_P — FUNC_TEST=TRUE — 52
BOARD_TEMP3_P — FUNC_TEST=TRUE — 52
BOARD_TEMP4_P — FUNC_TEST=TRUE — 52
BOARD_TEMP5_P — FUNC_TEST=TRUE — 52
BOARD_TEMP6_P — FUNC_TEST=TRUE — 52
BOARD_TEMP7_P — FUNC_TEST=TRUE — 52
BOARD_TEMP8_P — FUNC_TEST=TRUE — 52
TP_BUCK_LDO_UOV — FUNC_TEST=TRUE — 52
TP_BUCK_SLPD_MUX — FUNC_TEST=TRUE — 52
TP_AMUX_AY — FUNC_TEST=TRUE — 52
TP_AMUX_BY — FUNC_TEST=TRUE — 52

PP9511 1 DWI_SOC2PMU_CLK — NO_TEST=TRUE — 6 62
PP9512 1 DWI_SOC2PMU_DO — NO_TEST=TRUE — 6 62
PP95F1 1 SYS_ALIVE — 62

GRAPE

I2C_GRAPE_SDA_1V8 (CUMULUS TDO) — FUNC_TEST=TRUE — 29 30
TP_JTAG_CUMULUS_M_TCK — FUNC_TEST=TRUE — 30
TP_JTAG_CUMULUS_M_TDI — FUNC_TEST=TRUE — 30
JTAG_CUMULUS_M_TMS — FUNC_TEST=TRUE — 30
SPI_GRAPE_SCLK — FUNC_TEST=TRUE — 6 30
SPI_GRAPE_MISO — FUNC_TEST=TRUE — 6 30
SPI_GRAPE_MOSI — FUNC_TEST=TRUE — 6 30
SPI_GRAPE_CS_L — FUNC_TEST=TRUE — 6 30
GPIO_SOC2GRAPE_RESET_L — FUNC_TEST=TRUE — 6 30
GPIO_GRAPE2SOC_IRQ_L — FUNC_TEST=TRUE — 6 30
DISPLAY_SYNC — FUNC_TEST=TRUE — 6 30
CLK_SOC2GRAPE_32K — FUNC_TEST=TRUE — 9 30 69
CUMULUS_M2S_CLK — FUNC_TEST=TRUE — 30
CUMULUS_M2S_SDA — FUNC_TEST=TRUE — 30
I2C_GRAPE_SDA_1V8 — FUNC_TEST=TRUE — 29 30 70
I2C_GRAPE_SCL_1V8 — FUNC_TEST=TRUE — 29 30

PP9514 1 TP_CUMULUS_S_CS_L — 30
PP9515 1 TP_CUMULUS_S_GPIO_3 — 30

AUDIO

DMIC_MIC_SD — FUNC_TEST=TRUE — 22 23
DMIC_BTN_SD — FUNC_TEST=TRUE — 22 28
GPIO_CODEC2SOC_IRQ_L — FUNC_TEST=TRUE — 6 22

TP9500 A 1 TP-P5
TP9501 A 1 TP-P5 — SPKRAMP_R_OUT_P — FUNC_TEST=TRUE — 24 27 69
TP9502 A 1 TP-P5 — SPKRAMP_R_OUT_N — FUNC_TEST=TRUE — 24 27 69
TP9503 A 1 TP-P5
TP9510 A 1 TP-P5
TP9511 A 1 TP-P5 — SPKRAMP_L_OUT_P — FUNC_TEST=TRUE — 24 27 69
TP9512 A 1 TP-P5 — SPKRAMP_L_OUT_N — FUNC_TEST=TRUE — 24 27 69
TP9513 A 1 TP-P5

PP95D0 1 I2S_SOC2SPKRAMP_MCK — 6 24
PP95D1 1 I2S_SOC2SPKRAMP_BCLK — 6 24
PP95D2 1 I2S_SOC2SPKRAMP_LRCK — 6 24
PP95D3 1 I2S_SOC2SPKRAMP_DOUT — 6 24
PP95D4 1 I2S_SPKRAMP2SOC_DOUT — 6 24

PP95D7 1 I2S_SOC2CODEC_ASP_MCK — 6 22
PP95D8 1 I2S_SOC2CODEC_ASP_BCLK — 6 22
PP95D9 1 I2S_SOC2CODEC_ASP_LRCK — 6 22
PP95DA 1 I2S_SOC2CODEC_ASP_DOUT — 6 22
PP95DB 1 I2S_CODEC2SOC_ASP_DOUT — 6 22
PP95DC 1 I2S_SOC2CODEC_XSP_BCLK — 6 22
PP95DD 1 I2S_SOC2CODEC_XSP_LRCK — 6 22
PP95DE 1 I2S_SOC2CODEC_XSP_DOUT — 6 22
PP95DF 1 I2S_CODEC2SOC_XSP_DOUT — 6 22

CAMERA - FRONT

PP9520 1 MIPI_CAM_FRONT_CLK_P — PLACE_NEAR=U0600.AV36:3MM — NO_XNET_CONNECTION=TRUE — 8 21 70
PP9521 1 MIPI_CAM_FRONT_CLK_N — PLACE_NEAR=U0600.AW36:3MM — NO_XNET_CONNECTION=TRUE — 8 21 70
PP9522 1 MIPI_CAM_FRONT_DATA_P<0> — PLACE_NEAR=U0600.AV37:3MM — NO_XNET_CONNECTION=TRUE — 8 21 70
PP9523 1 MIPI_CAM_FRONT_DATA_N<0> — PLACE_NEAR=U0600.AW37:3MM — NO_XNET_CONNECTION=TRUE — 8 21 70

CAMERA - REAR

PP9524 1 MIPI_CAM_REAR_CLK_P — PLACE_NEAR=U0600.AV31:3MM — NO_XNET_CONNECTION=TRUE — 8 21 70
PP9525 1 MIPI_CAM_REAR_CLK_N — PLACE_NEAR=U0600.AW31:3MM — NO_XNET_CONNECTION=TRUE — 8 21 70
PP9526 1 MIPI_CAM_REAR_DATA_P<0> — PLACE_NEAR=U0600.AV33:3MM — NO_XNET_CONNECTION=TRUE — 8 21 70
PP9527 1 MIPI_CAM_REAR_DATA_N<0> — PLACE_NEAR=U0600.AW33:3MM — NO_XNET_CONNECTION=TRUE — 8 21 70

OSCAR

PP95C0 1 TP_OSCAR_P0_05 — 17
PP95C1 1 TP_OSCAR_P0_06 — 17
PP95C2 1 TP_OSCAR_P0_09 — 17
PP95C3 1 TP_OSCAR_P0_17 — 17
PP95C4 1 TP_OSCAR_P0_21 — 17
PP95C8 1 TP_OSCAR_P1_02 — 17
PP95C9 1 TP_OSCAR_P1_03 — 17
PP95CD 1 SWD_OSCAR_IO_1V8 — 9 17
PP95CF 1 SWD_OSCAR_CLK_1V8 — 9 17

CHAN 0 NEAR DRAM

PP9534 1 DDR0_CK_P — PLACE_NEAR=U1600.W13:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9535 1 DDR0_CK_N — PLACE_NEAR=U1600.W12:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9536 1 DDR0_CKE<0> — PLACE_NEAR=U1600.W14:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9537 1 DDR0_CA<0> — PLACE_NEAR=U1600.V17:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9538 1 DDR0_CA<1> — PLACE_NEAR=U1600.W17:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9539 1 DDR0_CA<2> — PLACE_NEAR=U1600.V16:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9540 1 DDR0_CA<3> — PLACE_NEAR=U1600.W16:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9541 1 DDR0_CSN<0> — PLACE_NEAR=U1600.Y14:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9530 1 DDR0_DQS_P<0> — PLACE_NEAR=U1600.D15:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9531 1 DDR0_DQS_N<0> — PLACE_NEAR=U1600.D14:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9532 1 DDR0_DQ<0> — PLACE_NEAR=U1600.C17:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70

CHAN 0 NEAR SOC

PP9570 1 DDR0_DQS_P<0> — PLACE_NEAR=U0600.D7:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9571 1 DDR0_DQS_N<0> — PLACE_NEAR=U0600.D6:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9572 1 DDR0_DQ<0> — PLACE_NEAR=U0600.F10:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70

CHAN 1 NEAR DRAM

PP9542 1 DDR1_DQS_P<0> — PLACE_NEAR=U1600.K4:1MM — NO_XNET_CONNECTION=TRUE — 70 10 14
PP9543 1 DDR1_DQS_N<0> — PLACE_NEAR=U1600.L4:1MM — NO_XNET_CONNECTION=TRUE — 70 10 14
PP9544 1 DDR1_DQ<0> — PLACE_NEAR=U1600.H3:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70

CHAN 1 NEAR SOC

PP9582 1 DDR1_DQS_P<0> — PLACE_NEAR=U0600.V1:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9583 1 DDR1_DQS_N<0> — PLACE_NEAR=U0600.U1:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70
PP9584 1 DDR1_DQ<0> — PLACE_NEAR=U0600.AA3:1MM — NO_XNET_CONNECTION=TRUE — 10 14 70

I2C

I2C_OSCAR2PROX_SDA_1V8 — FUNC_TEST=TRUE — 17 58
I2C_OSCAR2PROX_SCL_1V8 — FUNC_TEST=TRUE — 17 58
I2C0_SCL_1V8 — FUNC_TEST=TRUE — 4 6
I2C0_SDA_1V8 — FUNC_TEST=TRUE — 4 6
I2C1_SCL_1V8 — FUNC_TEST=TRUE — 4 6
I2C1_SDA_1V8 — FUNC_TEST=TRUE — 4 6
I2C2_SCL_1V8 — FUNC_TEST=TRUE — 4 6
I2C2_SDA_1V8 — FUNC_TEST=TRUE — 4 6

PP95F4 1 =I2C3_SDA_1V8 — 4
PP95F5 1 =I2C3_SCL_1V8 — 4

I2C_HP_ALS_SCL_1V8_FILT — FUNC_TEST=TRUE — 23 69
I2C_HP_ALS_SDA_1V8_FILT — FUNC_TEST=TRUE — 23 69
I2C_MIC_ALS_SCL_1V8_F — FUNC_TEST=TRUE — 23 69
I2C_MIC_ALS_SDA_1V8_F — FUNC_TEST=TRUE — 23 69

UART

UART_SOC2ACC_TX — FUNC_TEST=TRUE — 6 25
UART_ACC2SOC_TX — FUNC_TEST=TRUE — 6 25
UART_SOC2OSCAR_TX — FUNC_TEST=TRUE — 6 17
UART_OSCAR2SOC_TX — FUNC_TEST=TRUE — 6 17

CHAN 2 NEAR DRAM

PP9548 1 DDR2_CK_P — PLACE_NEAR=U1700.W13:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9549 1 DDR2_CK_N — PLACE_NEAR=U1700.W12:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9550 1 DDR2_CKE<0> — PLACE_NEAR=U1700.W14:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9551 1 DDR2_CA<0> — PLACE_NEAR=U1700.V17:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9552 1 DDR2_CA<1> — PLACE_NEAR=U1700.W17:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9553 1 DDR2_CA<2> — PLACE_NEAR=U1700.V16:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9554 1 DDR2_CA<3> — PLACE_NEAR=U1700.W16:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9555 1 DDR2_CSN<0> — PLACE_NEAR=U1700.Y14:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9545 1 DDR2_DQS_P<0> — PLACE_NEAR=U1700.D15:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9546 1 DDR2_DQS_N<0> — PLACE_NEAR=U1700.D14:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9547 1 DDR2_DQ<0> — PLACE_NEAR=U1700.C17:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70

CHAN 2 NEAR SOC

PP9585 1 DDR2_DQS_P<0> — PLACE_NEAR=U0600.AM1:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9586 1 DDR2_DQS_N<0> — PLACE_NEAR=U0600.AL1:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9587 1 DDR2_DQ<0> — PLACE_NEAR=U0600.AR3:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70

CHAN 3 NEAR DRAM

PP9556 1 DDR3_DQS_P<0> — PLACE_NEAR=U1700.K4:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9557 1 DDR3_DQS_N<0> — PLACE_NEAR=U1700.L4:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9558 1 DDR3_DQ<0> — PLACE_NEAR=U1700.H3:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70

CHAN 3 NEAR SOC

PP9596 1 DDR3_DQS_P<0> — PLACE_NEAR=U0600.AT10:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9597 1 DDR3_DQS_N<0> — PLACE_NEAR=U0600.AT11:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70
PP9598 1 DDR3_DQ<0> — PLACE_NEAR=U0600.AP7:1MM — NO_XNET_CONNECTION=TRUE — 10 15 70

WIFI

TP_JTAG_WLAN_TMS — FUNC_TEST=TRUE — 68
TP_JTAG_WLAN_TRST — FUNC_TEST=TRUE — 68
JTAG_WLAN_SEL (TDI) — FUNC_TEST=TRUE — 57
UART_SOC2WLAN_RTS_L (TDO) — FUNC_TEST=TRUE — 6 57 68
TP95B0 A 1 TP-P5 — WLAN_SECI_IN — FUNC_TEST=TRUE — 57
OSCAR2RADIO_CONTEXT_A — FUNC_TEST=TRUE — 57 68
OSCAR2RADIO_CONTEXT_B — FUNC_TEST=TRUE — 57 68
UART_BT2SOC_TX — FUNC_TEST=TRUE — 6 68
UART_SOC2BT_TX — FUNC_TEST=TRUE — 6 57 68
UART_SOC2WLAN_TX — FUNC_TEST=TRUE — 6 57 68
UART_WLAN2SOC_TX — FUNC_TEST=TRUE — 6 68
UART_BB2WLAN_COEX_RX — FUNC_TEST=TRUE — 40 57 71
UART_WLAN2BB_COEX_TX — FUNC_TEST=TRUE — 40 57 71
I2S_SOC2BT_BCLK — FUNC_TEST=TRUE — 6 57 68
I2S_SOC2BT_LRCK — FUNC_TEST=TRUE — 6 57 68
I2S_BT2SOC_DOUT — FUNC_TEST=TRUE — 6 68
I2S_SOC2BT_DOUT — FUNC_TEST=TRUE — 6 57 68
CLK_PMU2WLAN_32K — FUNC_TEST=TRUE — 57 62 68 69 70
GPIO_PMU2WLAN_REG_ON — FUNC_TEST=TRUE — 57 62 68 69
GPIO_PMU2BT_REG_ON — FUNC_TEST=TRUE — 57 62 68 69
GPIO_WLAN2PMU_HOST_WAKE — FUNC_TEST=TRUE — 57 62 68
GPIO_BT2PMU_HOST_WAKE — FUNC_TEST=TRUE — 57 62 68 70
GPIO_SOC2WLAN_WAKE — FUNC_TEST=TRUE — 9 68
GPIO_SOC2BT_WAKE — FUNC_TEST=TRUE — 9 57 68

OTHER PPS
PP95B8 1 WLAN_GPIO_8 — NO_TEST=TRUE — 57
PP95B9 1 WLAN_GPIO_16 — NO_TEST=TRUE — 57

PP95B5 1 UART_WLAN2SOC_RTS_L — 6 68
PP95B6 1 UART_BT2SOC_RTS_L — 6 68
PP95B7 1 UART_SOC2BT_RTS_L — 6 57 68

SOC SIDE PCIE TPS
PP95A0 1 PLACE_NEAR=U0600.D28:3MM — PCIE_WLAN2SOC_TX_P — 9 68 70
PP95A1 1 PLACE_NEAR=U0600.E28:3MM — PCIE_WLAN2SOC_TX_N — 9 68 70

REMOVED PCIE_SOC2WLAN_TX_C_P PP BECAUSE
THE IT BLOCKED THE SHIM RING.
REMOVED PCIE_SOC2WLAN_TX_C_N PP BECASUE
THE *_P VERSION WAS REMOVED

PP95A6 1 PLACE_NEAR=U0600.J40:3MM — PCIE_WLAN2SOC_CLKREQ_L — 9 68 70

WLAN SIDE PCIE TPS
PP95A7 1 PLACE_NEAR=U7500.73:3MM — PCIE_WLAN2SOC_TX_C_P — 68 70
PP95A8 1 PLACE_NEAR=U7500.74:3MM — PCIE_WLAN2SOC_TX_C_N — 68 70
PP95A9 1 PLACE_NEAR=U7500.77:3MM — PCIE_SOC2WLAN_TX_P — 9 57 68 70
PP95B0 1 PLACE_NEAR=U7500.76:3MM — PCIE_SOC2WLAN_TX_N — 9 57 68 70
PP95B1 1 PLACE_NEAR=U7500.71:3MM — PCIE_SOC2WLAN_CLK_P — 9 57 68 70
PP95B2 1 PLACE_NEAR=U7500.70:3MM — PCIE_SOC2WLAN_CLK_N — 9 57 68 70
PP95B3 1 PLACE_NEAR=U7500.81:3MM — PCIE_SOC2WLAN_RESET_L — 9 68 70

HIGH SPEED, NO TEST

DDR0_CA<0..9> — NO_TEST=TRUE — 10 14 70
DDR0_CK_P — NO_TEST=TRUE — 10 14 70
DDR0_CK_N — NO_TEST=TRUE — 10 14 70
DDR0_CA<0..9> — NO_TEST=TRUE — 10 14 70
DDR0_CKE<0..1> — NO_TEST=TRUE — 10 14 70
DDR0_CSN<0..1> — NO_TEST=TRUE — 10 14 70
DDR0_DM<0..3> — NO_TEST=TRUE — 10 14
DDR0_DQ<0..31> — NO_TEST=TRUE — 10 14 70
DDR0_DQS_P<0..3> — NO_TEST=TRUE — 10 14 70
DDR0_DQS_N<0..3> — NO_TEST=TRUE — 10 14 70
DDR1_CA<0..9> — NO_TEST=TRUE — 10 14 70
DDR1_CK_P — NO_TEST=TRUE — 10 14
DDR1_CK_N — NO_TEST=TRUE — 10 14
DDR1_CA<0..9> — NO_TEST=TRUE — 10 14 70
DDR1_CKE<0..1> — NO_TEST=TRUE — 10 14
DDR1_CSN<0..1> — NO_TEST=TRUE — 10 14
DDR1_DM<0..3> — NO_TEST=TRUE — 10 14
DDR1_DQ<0..31> — NO_TEST=TRUE — 10 14 70
DDR1_DQS_P<0..3> — NO_TEST=TRUE — 10 14 70
DDR1_DQS_N<0..3> — NO_TEST=TRUE — 10 14 70
DDR2_CA<0..9> — NO_TEST=TRUE — 10 15 70
DDR2_CK_P — NO_TEST=TRUE — 10 15 70
DDR2_CK_N — NO_TEST=TRUE — 10 15 70
DDR2_CA<0..9> — NO_TEST=TRUE — 10 15 70
DDR2_CKE<0..1> — NO_TEST=TRUE — 10 15 70
DDR2_CSN<0..1> — NO_TEST=TRUE — 10 15 70
DDR2_DM<0..3> — NO_TEST=TRUE — 10 15
DDR2_DQ<0..31> — NO_TEST=TRUE — 10 15 70
DDR2_DQS_P<0..3> — NO_TEST=TRUE — 10 15 70
DDR2_DQS_N<0..3> — NO_TEST=TRUE — 10 15 70
DDR3_CA<0..9> — NO_TEST=TRUE — 10 15 70
DDR3_CK_P — NO_TEST=TRUE — 10 15
DDR3_CK_N — NO_TEST=TRUE — 10 15
DDR3_CA<0..9> — NO_TEST=TRUE — 10 15 70
DDR3_CKE<0..1> — NO_TEST=TRUE — 10 15
DDR3_CSN<0..1> — NO_TEST=TRUE — 10 15
DDR3_DM<0..3> — NO_TEST=TRUE — 10 15
DDR3_DQ<0..31> — NO_TEST=TRUE — 10 15 70
DDR3_DQS_P<0..3> — NO_TEST=TRUE — 10 15 70
DDR3_DQS_N<0..3> — NO_TEST=TRUE — 10 15 70

MIPI_CAM_REAR_CLK_P — NO_TEST=TRUE — 8 21 70
MIPI_CAM_REAR_CLK_N — NO_TEST=TRUE — 8 21 70
MIPI_CAM_REAR_DATA_P<0..1> — NO_TEST=TRUE — 8 21 70
MIPI_CAM_REAR_DATA_N<0..1> — NO_TEST=TRUE — 8 21 70
MIPI_CAM_REAR_CLK_FILT_P — NO_TEST=TRUE — 20 21
MIPI_CAM_REAR_CLK_FILT_N — NO_TEST=TRUE — 20 21
MIPI_CAM_REAR_DATA_FILT_P<0..3> — NO_TEST=TRUE — 20 21
MIPI_CAM_REAR_DATA_FILT_N<0..3> — NO_TEST=TRUE — 20 21
MIPI_CAM_FRONT_CLK_P — NO_TEST=TRUE — 8 21 70
MIPI_CAM_FRONT_CLK_N — NO_TEST=TRUE — 8 21 70
MIPI_CAM_FRONT_DATA_P<0> — NO_TEST=TRUE — 8 21 70
MIPI_CAM_FRONT_DATA_N<0> — NO_TEST=TRUE — 8 21 70
MIPI_CAM_FRONT_CLK_FILT_P — NO_TEST=TRUE — 20 21
MIPI_CAM_FRONT_CLK_FILT_N — NO_TEST=TRUE — 20 21
MIPI_CAM_FRONT_DATA_FILT_P<0> — NO_TEST=TRUE — 20 21
MIPI_CAM_FRONT_DATA_FILT_N<0> — NO_TEST=TRUE — 20 21

EDP_DATA_P<0..3> — NO_TEST=TRUE — 9 32
EDP_DATA_N<0..3> — NO_TEST=TRUE — 9 32
EDP_DATA_EMI_P<0..3> — NO_TEST=TRUE — 32
EDP_DATA_EMI_N<0..3> — NO_TEST=TRUE — 32
EDP_DATA_EMI_CONN_P<0..3> — NO_TEST=TRUE — 31 32
EDP_DATA_EMI_CONN_N<0..3> — NO_TEST=TRUE — 31 32

PCIE_WLAN2SOC_TX_P — NO_TEST=TRUE — 9 68 70
PCIE_WLAN2SOC_TX_N — NO_TEST=TRUE — 9 68 70
PCIE_SOC2WLAN_TX_P — NO_TEST=TRUE — 9 57 68 70
PCIE_SOC2WLAN_TX_N — NO_TEST=TRUE — 9 57 68 70
PCIE_SOC2WLAN_CLK_P — NO_TEST=TRUE — 9 57 68 70
PCIE_SOC2WLAN_CLK_N — NO_TEST=TRUE — 9 57 68 70
PCIE_WLAN2SOC_TX_C_P — NO_TEST=TRUE — 68 70
PCIE_WLAN2SOC_TX_C_N — NO_TEST=TRUE — 68 70
PCIE_SOC2WLAN_TX_C_P — NO_TEST=TRUE — 9
PCIE_SOC2WLAN_TX_C_N — NO_TEST=TRUE — 9
PCIE_WLAN2SOC_CLKREQ_L — NO_TEST=TRUE — 9 68 70
PCIE_SOC2WLAN_RESET_L — NO_TEST=TRUE — 9 68 70

POWER, NO TEST

PP6V0_LCM_HI — NO_TEST=TRUE — 61 63
SW_CHGA — NO_TEST=TRUE — 65
WLED_LX_A — NO_TEST=TRUE — 61 63
WLED_LX_B — NO_TEST=TRUE — 61 63
L81_PVCP — NO_TEST=TRUE — 22
L81_NVCP — NO_TEST=TRUE — 22
L81_FLYC — NO_TEST=TRUE — 22
L81_FLYN — NO_TEST=TRUE — 22
L81_FLYP — NO_TEST=TRUE — 22

GRAPE NO_TEST
MT_PANEL_IN<0..29> — NO_TEST=TRUE — 29 30
MT_PANEL_OUT<0..39> — NO_TEST=TRUE — 29

SYNC_MASTER=N/A — SYNC_DATE=N/A
PAGE TITLE: TEST: EE TP/PP

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DRAWING NUMBER: 051-0301 — SIZE: D
REVISION: B.0.0
BRANCH
PAGE: 95 OF 155
SHEET: 70 OF 73

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RF TEAM REQUESTED TPS

SIMCRD_RST_CONN_FILT	FUNC_TEST=TRUE	59 69
SIMCRD_CLK_CONN_FILT	FUNC_TEST=TRUE	59 69
SIMCRD_IO_CONN_FILT	FUNC_TEST=TRUE	59 69
SIMCRD_DETECT_FILT	FUNC_TEST=TRUE	59 69
PP_LDO6	FUNC_TEST=TRUE	35 36 69 73
UART_BB2SOC_TX	FUNC_TEST=TRUE	6 25 68
UART_SOC2BB_TX	FUNC_TEST=TRUE	6 25 68
UART_BB2SOC_RTS_L	FUNC_TEST=TRUE	6 68
UART_SOC2BB_RTS_L	FUNC_TEST=TRUE	6 68
UART_OSCAR2BB_TX	FUNC_TEST=TRUE	17 68
UART_BB2OSCAR_TX	FUNC_TEST=TRUE	17 68
UART_BB2WLAN_COEX_RX	FUNC_TEST=TRUE	40 57 70
UART_WLAN2BB_COEX_TX	FUNC_TEST=TRUE	40 57 70
GPIO_SOC2BB_WAKE_MODEM	FUNC_TEST=TRUE	6 68
GPIO_BB2SOC_GPS_SYNC	FUNC_TEST=TRUE	6 68
USB_BB_P	FUNC_TEST=TRUE	25 68
USB_BB_N	FUNC_TEST=TRUE	25 68
GPIO_SOC2BB_COREDUMP	FUNC_TEST=TRUE	6 68
GPIO_SOC2BB_RADIO_ON_L	FUNC_TEST=TRUE	6 68 69
GPIO_PMU2BBPMU_RESET_L	FUNC_TEST=TRUE	62 68 69 70
GPIO_PMU2BB_VBUS_DET	FUNC_TEST=TRUE	62 68 69
PP9600 P4MM SM (PP) 1 HSIC_BB_DATA		5 68
PP9601 P4MM SM (PP) 1 HSIC_BB_STB		5 68

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REVISION: B.0.0

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PAGE: 96 OF 155

SHEET: 71 OF 73

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POWER CONNECTIONS

BUCK0 (DWI DVC)

69 60 PPVDD_CPU (MAKE_BASE=TRUE, VOLTAGE=1.1V) — =PPVDD_CPU 13

BUCK1 (DWI DVC)

69 60 PPVDD_GPU (MAKE_BASE=TRUE, VOLTAGE=1.1V) — =PPVDD_GPU 13

BUCK2

69 60 PP0V95_SOC (MAKE_BASE=TRUE, VOLTAGE=0.95V)
- =PP0V95_SOC 12
- =PP0V95_PCIE_SOC 9
- =PP0V95_USB_SOC 5

BUCK3

69 61 60 PP1V8_S2R (MAKE_BASE=TRUE, VOLTAGE=1.8V)
- =PP1V8_S2R_DDR 14 15
- =PP1V8_S2R_GRAPE_EXTERNAL_SW 30
- =PP1V8_S2R_TRISTAR 25
- =PP1V8_S2R_VDDIO_WLAN_BT 68
- =PP1V8_S2R_MISC 6 9 66 67
- =PP1V8_S2R_EXTERNAL_SW 64
- =PP1V8_S2R_ROTTERDAM 34

BUCK3_SW

BUCK3_SW1

69 67 60 PP1V8_SW1 (MAKE_BASE=TRUE, VOLTAGE=1.8V)
- =PP1V8_AUDIO 22 24
- =PP1V8_SW1_EXT_SW_ON 64
- XWC130 SM: 1 — 2 PP1V8_SW1_FOREHEAD 69 72

72 69 PP1V8_SW1_FOREHEAD (MAKE_BASE=TRUE, VOLTAGE=1.8V)
- =PP1V8_CAM_FRONT 21
- =PP1V8_CAM_REAR 21
- =PP1V8_DMIC 23 28

BUCK3_SW1_EXT

69 64 PP1V8_EXT_SW (MAKE_BASE=TRUE, VOLTAGE=1.8V)
- =PP1V8_VDDIO18_SOC 11
- =PP1V8_XTAL_SOC 11
- =PP1V8_PCIE_SOC 9
- =PP1V8_MIPI_SOC 8
- =PP1V8_NAND_SOC 7
- =PP1V8_NAND 16 70
- =PP1V8_NAND_EXT_SW_ON 64
- =PP1V8_SOC 4 5 6 62
- =PP1V8_EEPROM 6

BUCK3_SW2

69 60 PP1V8_SW2 (MAKE_BASE=TRUE, VOLTAGE=1.8V) — =PP1V8_SPKRAMP_DVDD 24

69 30 PP1V8_GRAPE_EXT_SW (MAKE_BASE=TRUE, VOLTAGE=1.8V) — =PP1V8_GRAPE_EXT_SW 29 30

BUCK3_SW3

69 60 PP1V8_S2R_SW3 (MAKE_BASE=TRUE, VOLTAGE=1.8V)
- =PP1V8_S2R_OSCAR 17
- =PP1V8_S2R_PHOS 18
- =PP1V8_S2R_GYRO 18
- =PP1V8_S2R_COMPASS 18
- =PP1V8_S2R_ACCEL 18
- =PP1V8_S2R_PROX 58

BUCK4

69 61 60 PP1V2_S2R (MAKE_BASE=TRUE, VOLTAGE=1.2V)
- =PP1V2_EXTERNAL_SW 64
- =PP1V2_S2R_DDR 14 15
- =PP1V2_S2R_DDR_SOC 10

BUCK4_SW1

69 60 PP1V2_SW1 (MAKE_BASE=TRUE, VOLTAGE=1.2V) — =PP1V2_EXT_SW_ON 64

69 64 PP1V2_EXT_SW (MAKE_BASE=TRUE, VOLTAGE=1.2V)
- =PP1V2_DDR_VDDQ 14 15
- =PP1V2_VDDIOD_SOC 10 11
- =PP1V2_HSIC_SOC 5
- =PP1V2_PLL_SOC 9 11
- =PP1V2_CAM_FRONT 21

BUCK4_SW2

69 60 PP1V2_S2R_SW2 (MAKE_BASE=TRUE, VOLTAGE=1.2V) — =PP1V2_S2R_OSCAR 17

BUCK5 (DWI DVC)

69 60 PPVDD_SRAM (MAKE_BASE=TRUE, VOLTAGE=1.1V) — =PPVDD_SRAM 13

BUCK6

69 60 PP3V3_S2R (MAKE_BASE=TRUE, VOLTAGE=3.3V)
- =PP3V3_S2R_EXTERNAL_SW 64
- =PP3V3_S2R_WIFI_PA 68

69 64 PP3V3_EXT_SW (MAKE_BASE=TRUE, VOLTAGE=3.3V)
- =PP3V3_NAND 16
- =PP3V3_USB_SOC 5

LDO1

69 61 PP3V0_S2R_HALL (MAKE_BASE=TRUE, VOLTAGE=3.0V) — =PP3V0_S2R_HALL 19 30

LDO2

69 61 PP1V7_VA_VCP (MAKE_BASE=TRUE, VOLTAGE=1.7V) — =PP1V7_VA_VCP 22

LDO3

69 61 PP3V0_S2R_SENSOR (MAKE_BASE=TRUE, VOLTAGE=3.0V)
- =PP3V0_S2R_PROX 58
- =PP3V0_S2R_COMPASS 18
- =PP3V0_S2R_GYRO 18

LDO4

69 61 PP3V0_ALS (MAKE_BASE=TRUE, VOLTAGE=3.0V)
- =PP3V0_HP_ALS 23
- =PP3V0_MIC_ALS 23

LDO5

69 61 PP3V1_S2R_MESA (MAKE_BASE=TRUE, VOLTAGE=3.1V) — =PP3V1_S2R_MESA 33

LDO6

69 61 PP3V3_ACC (MAKE_BASE=TRUE, VOLTAGE=3.3V) — =PP3V3_ACC 25

LDO7

69 61 PP3V0_S2R_TRISTAR (MAKE_BASE=TRUE, VOLTAGE=3.0V)
- =PP3V0_S2R_TRISTAR 25
- =PP3V0_S2R_ANT_SW 59

LDO8

72 69 61 PP3V0_MISC (MAKE_BASE=TRUE, VOLTAGE=3.0V) — PP3V0_MISC 61 69 72

LDO9

69 61 PP1V25_CAM (MAKE_BASE=TRUE, VOLTAGE=1.25V) — =PP1V25_CAM_REAR 21

LDO10

69 61 PP1V0_SOC (MAKE_BASE=TRUE, VOLTAGE=1.0V)
- =PP1V0_MIPI_SOC 8
- =PP1V0_LPDP_SOC 9

LDO11

69 61 PP2V6_CAM_AF (MAKE_BASE=TRUE, VOLTAGE=2.6V) — =PP2V6_CAM_REAR_AF 21

LDO13

69 61 PP2V9_CAM (MAKE_BASE=TRUE, VOLTAGE=2.9V)
- =PP2V9_CAM_FRONT 21
- =PP2V9_CAM_REAR 21

LDO14

72 69 61 PP1V8_SPARE (MAKE_BASE=TRUE, VOLTAGE=1.8V) — PP1V8_SPARE 61 69 72

VLCM1

69 61 PP5V25_GRAPE (MAKE_BASE=TRUE, VOLTAGE=5.25V) — =PP5V25_GRAPE 29 30

CHARGER MAIN

69 65 64 61 60 PPVCC_MAIN (MAKE_BASE=TRUE, VOLTAGE=4.7V)
- =PPVCC_MAIN_AUDIO 22
- =PPVCC_MAIN_LED 63
- =PPVCC_MAIN_CPU 60
- =PPVCC_MAIN_GPU 60
- =PPVCC_MAIN_SOC 60
- =PPVCC_MAIN_GRAPE 29 30
- =PPVCC_MAIN_LCD 32
- =PPVCC_MAIN_VDD_LCM 61
- =PPVCC_MAIN_WLAN 68
- =PPVCC_MAIN_MESA 33
- =PPVCC_MAIN_ROTTERDAM 34

BATTERY

69 65 60 PPBATT_VCC (MAKE_BASE=TRUE, VOLTAGE=4.7V)
- =PPBATT_POS_CONN 66
- =PPBATT_VCC_BB 68
- =PPBATT_AUDIO 24

USB POWER INPUT

69 65 PPVBUS_USB_DCIN (MAKE_BASE=TRUE, VOLTAGE=16V) — =PPVBUS_USB_EMI 26

ON_BUF

69 61 PP1V8_ALWAYS (MAKE_BASE=TRUE, VOLTAGE=1.8V) — =PP1V8_ALWAYS 6 11 62

BACKLIGHT BOOST

69 63 PPLED_OUT_A (MAKE_BASE=TRUE, VOLTAGE=20.4V) — =PPLED_REG_A 32

69 63 PPLED_OUT_B (MAKE_BASE=TRUE, VOLTAGE=20.4V) — =PPLED_REG_B 32

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: POWER: ALIASES

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DRAWING NUMBER: 051-0301 SIZE: D

REVISION: B.0.0

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PAGE: 121 OF 155

SHEET: 72 OF 73

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1.225V	PP_LDO1	36 38 42 43
1.8V	PP_LDO2	36 38
1.8V	PP_LDO3	36 37 38 55
3.075V	PP_LDO4	36 38
2.85V	PP_LDO5	36 38 59
2.85V	PP_LDO6	35 36 69 71
1.9V	PP_LDO7	36 38 40
2.05V	PP_LDO8	36 42 43
1.2V	PP_LDO9	36 38
0.9V	PP_LDO10	36 38
1.8V	PP_LDO11	35 36 38 39 40 42 43 44
0.95V	PP_LDO12	36 38
2.95V	PP_LDO13	36 38 55 69
2.95V	PP_LDO13_GPS	55
2.7V	PP_LDO14_RFSW	36 46 47
0.95V	VREG_SMPS3_0V95	36 69
2.075V	VREG_SMPS4_2V075	36

0.9V	PP_VSW_S1	36
1.25V	PP_VSW_S2	36
0.95V	PP_VSW_S3	36
2.075V	PP_VSW_S4	36

4.7V	PP_BATT_VCC	35 44 53 68
4.7V	PP_VCC_MAIN	73
4.2V	PP_BATT_VCC_2GPA	45
4.2V	PP_BATT_VCC_QPOET	44 45 50 51
4.2V	PP_BATT_VCC_RADIO	35 36
4.7V	PP_BATT_VCC_DSM	53
4.2V	PP_BATT_VCC_QPOET_HBS	51
4.2V	PP_BATT_VCC_QPOET_ASM	50
1.8V	PP_1V8_S2R_VDDIO_WLAN_BT	57 68
1.8V	PP_WL_VDDIO	57
4.7V	PP_VCC_MAIN	73

0V	S1_GND	36
0V	S2_GND	36
0V	S3_GND	36
0V	S4_GND	36
0V	GND_SW	44
0V	VOUT_BOOST_GND	44

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PAGE TITLE
BB/WLAN VOLTAGE ATTRIBUTES

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PAGE 155 OF 155

SHEET 73 OF 73

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